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Optical network-on-chip (ONoC) architectures: a detailed analysis of optical router designs

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Abstract: Optical network-on-chip (ONoC) systems have emerged as a promising solution to overcome limitations of traditional electronic interconnects. Efficient ONoC architectures rely on optical routers, enabling high-speed data transfer, efficient routing, and scalability. This paper presents a comprehensive survey analyzing optical router designs, specifically microring resonators (MRRs), Mach–Zehnder interferometers (MZIs), and hybrid architectures. Selected comparison criteria, chosen for their critical importance, significantly impact router functionality and performance. By emphasizing these criteria, valuable insights into the strengths and limitations of different designs are gained, facilitating informed decisions and advancements in optical networking. While other factors contribute to performance and efficiency, the chosen criteria consistently address fundamental elements, enabling meaningful evaluation. This work serves as a valuable resource for beginners, providing a solid foundation in understanding ONoC and optical routers. It also offers an in-depth survey for experts, laying the groundwork for further exploration. Additionally, the importance of considering design constraints and requirements when selecting an optimal router design is highlighted. Continued research and innovation will enable the development of efficient optical router solutions that meet the evolving needs of modern computing systems. This survey underscores the significance of ongoing advancements in the field and their potential impact on future technologies.

Key words: optical network-on-chip (ONoC); optical routers; microring resonators (MRRs); Mach–Zehnder interferometers (MZIs); optical networking scalability

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1. Introduction

In modern system on chip (SoC) architectures, the increasing demand for computational power necessitates the integration of a larger number of processing cores. To efficiently manage inter core communication, NoC architectures have been developed. However, traditional electrical interconnects are increasingly unable to meet the rigorous demands for power efficiency, bandwidth, and scalability as the number of cores expands[1, 2]. This limitation is further compounded by the deceleration of Moore's Law, which has historically driven the exponential growth in transistor density. As the benefits of continued transistor scaling diminish, alternative technologies are needed to address these emerging challenges.

Optical networks on chip (ONoC) have emerged as a significant alternative to traditional electrical interconnects, leveraging the high speed and broad bandwidth characteristics of optical communication. This shift to photonic technologies addresses the limitations faced by electrical interconnects and provides a pathway for continued performance improvements in high-density computing environments.

Central to the efficacy of ONoC are optical routers, which play a pivotal role in the overall performance and scalability of these networks. Optical routers are responsible for directing optical signals between processing cores, performing essential functions that ensure efficient data transmission. These functions include managing the routing of signals, optimizing data paths to mitigate congestion, and minimizing latency. The ability of optical routers to efficiently handle high data rates and complex traffic patterns is critical for maintaining the performance of large scale ONoC systems.

A key feature of optical routers is their capability to support wavelength division multiplexing (WDM), a technique that enables the simultaneous transmission of multiple data streams over different wavelengths of light. This multiplexing capability significantly enhances the network's bandwidth and throughput, allowing ONoC to accommodate higher core counts and increased data traffic without degradation in performance[3–7]. By managing multiple wavelengths effectively, optical routers facilitate the scalability of ONoC, making them suitable for future computing architectures.

In addition to bandwidth management, optical routers contribute to power efficiency, a critical consideration in modern computing systems. Traditional electrical interconnects face substantial power dissipation issues, which are exacerbated by the increasing data rates and core densities. Optical routers, by utilizing optical signals, reduce power consumption compared to electrical alternatives[8–10]. This reduction in power dissipation is achieved through lower energy requirements for signal transmission and minimal heat generation. Furthermore, optical communication is less prone to electromagnetic interference, which can adversely affect signal integrity in electrical systems. This inherent immunity to interference enhances the reliability and robustness of ONoC.

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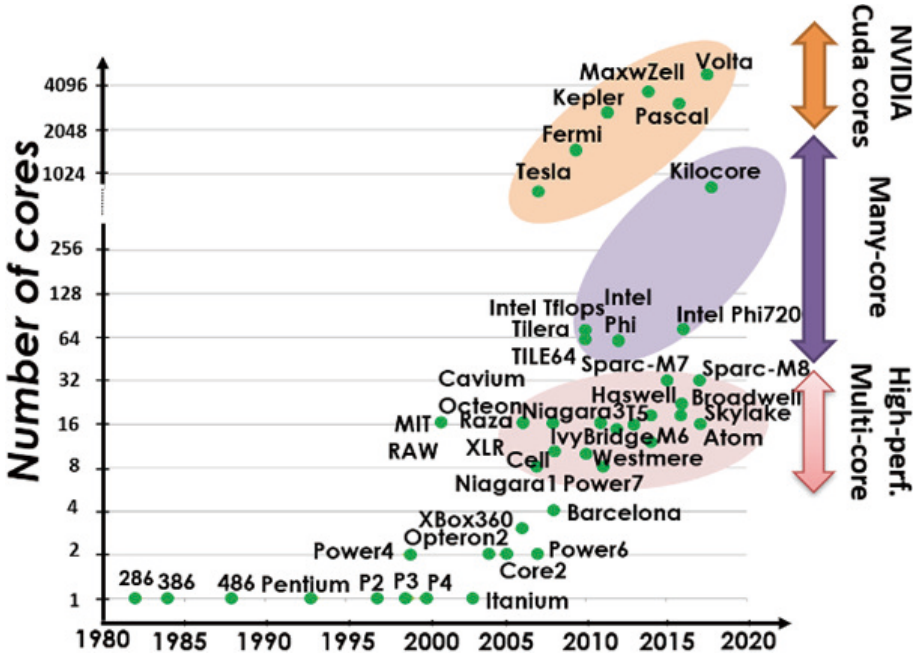

Fig. 1. (Color online) Evolution from single to many core computing architectures[12].

Given the constraints of electrical interconnects and the pressing need for efficient, high bandwidth communication solutions, optical routers represent a critical advancement in the design of ONoC. Their development is essential for overcoming the limitations of traditional technologies and enabling continued progress in high performance computing. The advancements in optical router technology are fundamental to improving the performance, scalability, and energy efficiency of ONoC.

This survey focuses on the design and functionality of optical routers, underscoring their importance within photonic network architectures. By providing a detailed examination of recent advancements and current research in optical router technology, this paper aims to justify the significant research investment in this area and highlight the profound impact of optical routers on enhancing the capabilities of ONoC.

2. Motivation and survey organization

This research is driven by the transformative potential of optical (NoC) technology, which promises to revolutionize computing systems such as next generation servers, data centers, and processors. The semiconductor industry is exploring photonics based processors as a compelling solution, demonstrating notable practical results[7].

In this context, optical routers are crucial. They are central to ONoC architectures, significantly influencing the system's performance, scalability, and efficiency. Beyond merely routing data traffic between cores, optical routers optimize overall system performance by minimizing latency, reducing power consumption, and managing high bandwidth demands. While routers have always been vital in traditional NoC systems, their role becomes even more critical in photonic NoC systems, where the rise in core counts necessitates advanced data routing mechanisms. This survey focuses on the exploration of optical routers to achieve enhancements in ONoC performance[11].

Traditional electrical NoC face limitations in power efficiency, bandwidth, and scalability, which are increasingly inadequate given the demands of modern multicore systems. As core counts rise, these limitations highlight the need for alternative interconnect technologies. Photonic communication has emerged as a promising solution, offering higher data transmission speeds, greater bandwidth, and lower power dissipation compared to electronic counterparts. However, the effective implementation of photonic communication relies heavily on the performance of optical routers, which are essential for managing complex routing tasks. Thus, advancing optical routers is critical for realizing the full potential of ONoC and ensuring their viability as scalable solutions for high performance computing.

Fig. 1 depicts the evolution from single core to many core computing architectures. This visual representation highlights the growing complexity of interconnect systems and underscores the need for sophisticated and efficient routing mechanisms in ONoC[12].

Fig. 2 shows the evolution of optical communication over the past four decades. The chart not only illustrates rapid advancements in optical communication but also the significant milestones achieved in research and development. This progression emphasizes the importance of optical routers in maintaining the efficiency and scalability of photonic communication systems[11].

Fig. 3 provides a hierarchical view of photonic architectures, illustrating the crucial role of routers within the protocol layer. This chart highlights how routers are interrelated with other components, emphasizing their essential function in managing data flow and ensuring network performance[7, 13, 14].

This survey aims to address the need for a comprehensive analysis of optical router technology, capturing both the latest innovations and fundamental principles. It will provide valuable insights into the role of optical routers within ONoC architectures, serving as a resource for researchers and practitioners.

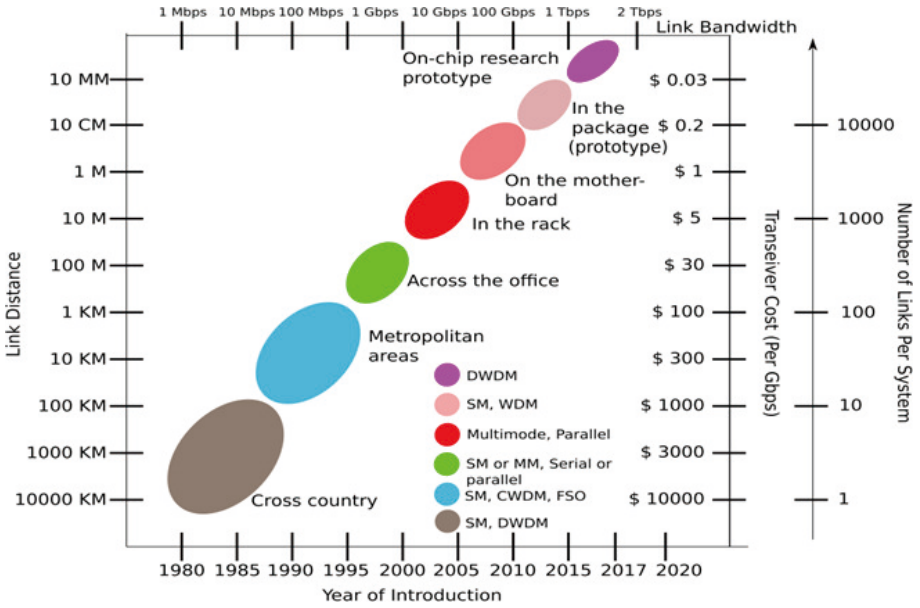

Fig. 2. (Color online) Optical communication evolution[11].

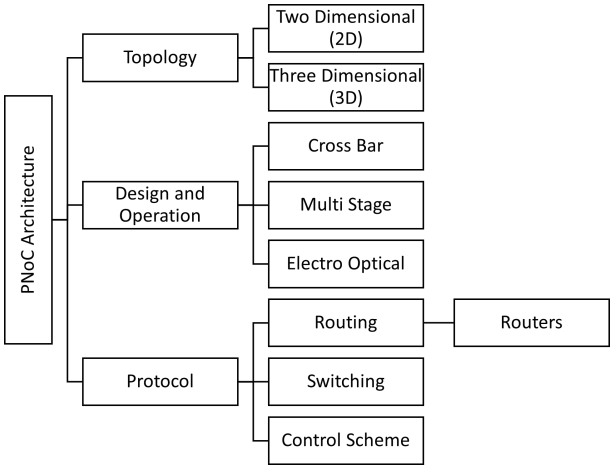

Fig. 3. Router concept relation in photonic architecture hierarchy[7].

3. Silicon photonics: towards efficient integrated optical systems

The evolution of photonic integrated circuit (PIC) technology, originating in the 1980s, has naturally progressed towards the realm of silicon photonics, where the utilization of optical waveguides on a PIC enables the intricate processing and efficient routing of light within the confines of a chip. Within the broad domain of PICs, various material systems, such as doped glass, $\mathrm{III}-\mathrm{V}$ semiconductors, polymers, and silicon, are currently employed, each offering distinct advantages and capabilities that cater to specific requirements and applications. Notably, among these material systems, silicon stands out in the silicon-on-insulator (SOI) platform due to its exceptional refractive index contrast, which facilitates the effective confinement of light within submicron waveguide cores and empowers precise bending of light with radii as small as a few micrometers[15].

Consequently, the integration of a myriad of functional optical building blocks onto a single chip becomes a feasible endeavor, opening up vast possibilities for advanced on-chip photonic systems. In striking contrast to the realm of complementary metal–oxide–semiconductor (CMOS) electronics, where a combination of transistors, resistors, diodes, and capacitors fulfills diverse functions, the fundamental components of a PIC exhibit significant diversity and impose a range of distinct requirements. As a foundational step, the implementation of low loss waveguides assumes a pivotal role in guiding the propagation of light, ensuring efficient signal transmission.

Moreover, effective splitters and precisely engineered waveguide crossings become essential elements for seamless distribution and optimal routing of light signals within the chip. However, the coupling of light between on-chip waveguides and optical fibers poses a notable challenge, primarily due to the polarization sensitivity often exhibited by on-chip waveguides, while optical fibers can accommodate two distinct polarization states of light. This disparity necessitates meticulous design and engineering considerations to achieve efficient and reliable coupling mechanisms. The diverse nature of light, characterized by its numerous wavelengths or, in other words, its expansive spectrum, further underscores the complexity of photonic systems.

In response to this, the majority of PIC technologies are designed to support the telecom wavelength bands between 1310 and 1550 nm in the near-infrared region. Accommodating this diverse range of wavelengths necessitates the integration of effective wavelength filters, such as optical delay lines or resonators, to enable applications in wavelength division multiplexed (WDM) communication, sensing, or spectroscopy[16].

These filters play a crucial role in selectively manipulating and routing specific wavelength channels, facilitating efficient and robust photonic signal processing. Intrinsic to the core operations of a PIC is the crucial process of opto–electronic conversion, which serves as a fundamental bridge between optical and electrical domains. In the context of silicon photonics, this conversion is achieved through the integration of a photodiode, typically implemented using germanium. The photodiode enables the conversion of incoming optical signals into corresponding electrical signals, facilitating seamless interaction with electronic components[17].

Additionally, leveraging the integration of a diode or

capacitor within a silicon waveguide, electrical signals can be impressively imprinted onto an optical carrier using either phase or amplitude modulation techniques, ensuring effective transmission and manipulation of information within the photonic system[18]. However, it is important to note that in silicon-based systems, the light source necessitates either bonding or off-chip coupling. Notably, lasers, serving as exemplary light sources, can be integrated monolithically within $\mathrm{III}-\mathrm{V}$ technology platforms, offering seamless integration and superior performance. Leveraging the well-established infrastructure and manufacturing techniques pioneered in CMOS electronics, the fabrication of silicon photonics now benefits from advanced manufacturing capabilities capable of defining deep submicron features with unprecedented accuracy and scalability. The underlying base material of silicon allows for the reuse of manufacturing tools, ensuring efficiency and cost effectiveness. Nevertheless, it is crucial to recognize that the integration of photonics imposes distinct requirements on fabrication processes.

Waveguides and transistors may require different layer thicknesses, and achieving optimal optical quality, such as mitigating unwanted absorption and minimizing scattering induced by surface roughness, emerges as a critical consideration. Consequently, the fabrication process must adhere to stringent nanometer scale tolerances to accommodate the extreme sensitivity of silicon photonic waveguides. Moreover, the precise fabrication of wavelength selective filters, conforming to stringent specifications[19], proves to be a formidable challenge due to the inherent variability induced by the fabrication process, necessitating the incorporation of active compensation mechanisms to ensure precise and reliable functionality. The integration of photonics with electronics assumes paramount importance in the context of driving and controlling functions within PICs.

This integration can be achieved through monolithic approaches, involving the seamless integration of optical and electrical components within a single wafer scale process[20], or through hybrid or three dimensional integration methods that capitalize on the complementary strengths of various fabrication techniques. As photonic chips continue to evolve and become increasingly sophisticated, the integration of electronic functions becomes even more vital, placing new and complex demands on the design aspects[21]. Consequently, ongoing research and development efforts strive to foster synergistic advancements in both the photonics and electronics domains, with a focus on seamless integration, improved performance, and enhanced functionalities within the realm of PICs.

Overcoming photonic interconnection challenges. Silicon photonics is set to revolutionize chip performance, driven by the demand for faster interconnection speeds. Nano photonics has emerged as a leading solution, with impressive advancements in optical communications, storage, sensors, biomedical devices, and other applications[22].

Photonic based platforms offer immense potential to enhance interconnection performance. However, they face fundamental challenges, such as the high cost of photonic components, assembly, and compatibility, which hinder their widespread implementation. Overcoming these obstacles necessitates a cost-effective approach capable of surmounting the bottlenecks encountered in the traditional integrated circuit industry. This approach must deliver high performance across a wide range of applications. Exploiting the advantages of silicon photonics provides a promising avenue to address these challenges and achieve significant breakthroughs in interconnection systems. Although progress has been made, optical interconnection systems still confront minor yet consequential issues.

These include low propagation loss, high bandwidth requirements, wavelength multiplexing, and immunity to electromagnetic noise[22]. Given the remarkable level of integration attained in silicon microelectronics and the shift from wire communication to optical fiber transmission, there arises a pressing need to combine optical waveguide transmission with dependable system integration on a silicon wafer scale. This integration holds immense potential for optimizing the performance of optical interconnection systems.

4. Silicon photonics: an overview and the basics of photonic interconnections

4.1. Challenges and comprehensive solutions in photonic interconnection

The high financial costs associated with photonic components, which include expenses related to fabrication, materials, and assembly, present significant barriers to their widespread adoption. The production of photonic devices often requires precision manufacturing techniques and costly materials, contributing to their elevated costs[23–26]. Several strategies are being explored to address these challenges:

Researchers are investigating less expensive substrates, such as polymers or silicon-on-insulator (SOI) wafers, to reduce overall costs[25–27].

Innovations in wafer scale integration and mass production methods have the potential to lower per-unit costs significantly, making photonic technologies more economically viable[25–27].

Development of materials like polymer waveguides or silicon nitride, which offer lower costs while maintaining or enhancing performance, is another key strategy[27].

These materials are expected to deliver similar or improved functionality at reduced costs.

Increasing production volumes can lower per-unit costs through economies of scale. Additionally, collaboration with industry partners and investment in advanced manufacturing infrastructure can support cost reduction efforts[28].

4.2. Integration and compatibility issues

Integrating photonic components with existing electronic systems introduces significant compatibility and performance challenges. Ensuring seamless operation between optical and electronic components requires overcoming issues related to precise alignment, signal interfacing, and power consumption[29].

Several approaches are being pursued to address these integration challenges:

Developing methods to integrate photonic devices with electronic circuits on the same chip or through advanced packaging techniques, such as flip–chip bonding and micro optics integration, is crucial for enhancing compatibility[25, 27–30].

Establishing standardized platforms that accommodate

both photonic and electronic components is essential for streamlining the integration process. These platforms provide a cohesive framework for integration, improving overall system performance[31].

Implementing precise alignment technologies and designing efficient optical-to-electrical interfaces are vital for enhancing the reliability and efficiency of hybrid systems. These technologies ensure accurate alignment and effective interaction between optical and electronic components[31].

4.3. Propagation loss and bandwidth requirements

Photonic interconnection systems must address challenges related to propagation loss and bandwidth requirements. High propagation loss can degrade signal quality, while meeting the high bandwidth demands of modern systems is crucial for maintaining optimal performance[31]. Researchers are focusing on several strategies to address these issues:

Creating innovative waveguide structures and materials, such as photonic crystal waveguides and low loss materials like silicon nitride, aims to minimize propagation loss and enhance signal quality[31].

Implementing WDM techniques can greatly increase bandwidth by enabling the simultaneous transmission of multiple data channels over different wavelengths, addressing the high bandwidth requirements of contemporary systems[31].

Using optical amplifiers and signal regeneration techniques is essential for maintaining signal strength over long distances and mitigating signal loss. These technologies ensure that signals remain strong and reliable as they travel through photonic interconnection systems[31].

4.4. Wavelength multiplexing and electromagnetic noise immunity

Efficient wavelength multiplexing and robust immunity to electromagnetic noise are crucial for ensuring the reliability of optical communication systems. While wavelength multiplexing is essential for increasing data throughput, it introduces complexities that must be managed to avoid performance degradation. Additionally, optical systems need effective shielding from electromagnetic interference (EMI), which can significantly impact system performance[31]. Key strategies to address these challenges include:

Improving WDM technology to support more channels while minimizing crosstalk and interference is crucial. Techniques such as dense wavelength division multiplexing (DWDM) play an instrumental role in increasing channel density and data rates, thus enabling more efficient use of the optical spectrum[31–34].

Implementing advanced shielding techniques to protect optical systems from EMI involves using materials with high electromagnetic shielding effectiveness and proper device encapsulation. These measures are essential for maintaining the integrity and reliability of optical communications by mitigating the effects of external electromagnetic disturbances[31–35].

4.5. System integration on a silicon wafer scale

Integrating optical waveguide transmission on a silicon wafer scale presents complex challenges related to precision and reliability. Successfully integrating optical components on a single wafer is critical for optimizing overall system performance and efficiency[31, 36]. Effective solutions being explored include:

Developing high precision manufacturing techniques and advanced alignment technologies, such as direct wafer bonding and laser assisted processes, is essential for improving integration accuracy and reliability. These innovations are crucial for maintaining the performance and integrity of photonic integrated circuits (PICs)[37].

Incorporating photonic components into system-on-chip (SoC) designs facilitates seamless integration and enhances overall system performance. This approach requires significant advancements in design and fabrication processes to achieve high density integration, which is essential for optimizing the performance of photonic systems[37]. System-on-chip designs enable more compact and efficient systems, paving the way for advanced applications in optical communication and computing.

4.6. Waveguides: fundamental components in silicon photonics

Waveguides are fundamental components in silicon photonics, serving as the primary conduits for guiding optical signals across photonic integrated circuits (PICs). Analogous to electrical wires in traditional electronic circuits, waveguides are designed to handle light rather than electrical currents. They come in various forms, each serving specific roles in signal transmission and routing:

Provide a direct, linear path for optical signals, facilitating straightforward transmission between components. Their design is optimized for efficient signal propagation over long distances without significant loss or distortion.

Enable the steering of light around corners and obstacles, allowing for complex routing within a photonic chip. This capability is essential for managing the spatial constraints of dense photonic circuits and ensuring effective signal delivery to various parts of the chip.

Transfer light between adjacent waveguides, allowing for signal sharing and interaction. This functionality is crucial for constructing intricate optical networks where signals need to be exchanged or combined at different points within the circuit.

At intersections where multiple waveguides converge, crossings must be carefully engineered to manage signal overlap and minimize losses and crosstalk. Proper design of waveguide crossings is essential for maintaining the overall performance and reliability of the photonic system.

Each type of waveguide plays a specific role in the design and optimization of photonic interconnections, contributing to the overall functionality of silicon photonics systems. Effective waveguide design is crucial for maintaining signal integrity, reducing propagation losses, and accommodating high data transfer rates in integrated photonic systems. By ensuring efficient signal transmission and routing, waveguides enable high speed data transfer and complex signal processing within photonic integrated circuits.

4.7. Optical couplers

Efficiently coupling light from optical fibers to photonic integrated circuits (PICs) remains a critical challenge in silicon photonics, primarily due to the significant refractive index contrast between the core and cladding materials of the silicon-on-insulator (SOI) platform. This contrast results in

single mode waveguides that are approximately 10^{-3} times smaller in cross sectional area compared to standard single mode fibers, leading to substantial coupling losses. Addressing these losses requires the development of highly effective coupling structures that are compact, offer broadband performance, and are cost effective to fabricate. Such structures are essential for seamless integration between silicon PICs and external optical fibers.

In silicon photonics, most applications require a very small optical mode size for single mode operation, exploiting the high index contrast between the silicon core and the silicon dioxide cladding. Thus, achieving efficient light coupling from optical fibers to PICs is of paramount importance. Couplers are critical components that facilitate the physical interface between on-chip components and off chip fibers[35]. However, developing effective coupling techniques involves overcoming challenges such as insertion loss, integration density, bandwidth density, crosstalk, reflectivity, and scalability.

To address these challenges, various innovative coupling techniques have been developed, employing both lateral and vertical approaches. The lateral coupling technique aligns the waveguide on the photonic chip laterally with the external optical fiber, often using grating couplers or tapered waveguides to achieve efficient light transfer. This method is particularly advantageous when lateral alignment is crucial, offering solutions that facilitate precise alignment and effective coupling.

Conversely, the vertical coupling technique focuses on achieving efficient light coupling through vertical alignment between the fiber and the photonic chip. This approach incorporates vertical structures, such as fiber to chip couplers or evanescent couplers, to enable effective light transfer. Vertical coupling techniques are especially effective when vertical alignment is critical, providing solutions that optimize light coupling by addressing vertical alignment challenges.

Both lateral and vertical coupling techniques aim to optimize the interface between the external optical fiber and the photonic chip, ensuring efficient light transmission and minimizing coupling losses. These techniques represent innovative solutions to the challenges of coupling light into and out of silicon photonic devices, enhancing their performance and expanding the potential applications of silicon photonics technology.

Additionally, corresponding optical packaging methods are essential to ensure optimal performance, reliability, and scalability of the coupled system. Effective optical packaging supports the practical implementation of these coupling techniques in real world applications, further improving the efficiency and reliability of silicon photonics systems[35, 38]. Therefore, ongoing advancements in both coupling techniques and packaging methods are crucial for the continued progress and broader adoption of silicon photonics technology.

4.8. Microring resonators in photonics NoC

The development of microring resonators represents a pivotal advancement in integrated photonics, significantly evolving over the past several decades. This progress is primarily due to the continuous refinement of sophisticated fabrication techniques[36]. Microring resonators, also known as ring resonators, have garnered substantial attention within the integrated photonics community due to their remarkable versatility, compact size, and compatibility with complementary metal–oxide–semiconductor (CMOS) technology. First proposed by Marcatili in 1969 at Bell Labs[37], microring resonators are valued for their ability to implement various networking functions efficiently while maintaining a compact footprint, making them essential components in photonic interconnection networks[39–44].

Microring resonators offer several advantages for on-chip optical integration. Unlike other optical feedback mechanisms that rely on mirrors or gratings, microring resonators simplify the manufacturing process by eliminating these additional components, thus enhancing scalability and cost effectiveness. They operate as traveling wave resonators with distinct optical paths for input, transmission, and reflection, which enables seamless compatibility with various optical elements such as waveguides, modulators, and detectors. This characteristic enhances the performance and functionality of integrated photonic systems.

Strategic coupling of multiple microring resonators, whether in series or parallel configurations, provides significant benefits for dense wavelength division multiplexing (DWDM) systems. This configuration allows a DWDM system to achieve a box like response and a broad free spectral range (FSR), facilitating the simultaneous transmission and processing of multiple wavelengths. Consequently, this arrangement substantially increases the data carrying capacity and spectral efficiency of optical communication systems.

The silicon-on-insulator (SOI) platform is highly promising for optical integration due to its high index contrast, which enables the fabrication of compact optical devices. SOI's compatibility with CMOS processes further enhances its appeal for integrated photonics applications. The advancements in microring resonators during the early twenty first century have solidified their role in silicon photonics, offering distinct advantages over alternatives such as distributed Bragg reflectors and facet mirrors. Their integration into planar silicon microelectronics is relatively straightforward, simplifying incorporation into existing systems. Moreover, microring resonators offer versatile integration possibilities with other critical components, such as waveguides, mirrors, and Mach–Zehnder interferometers (MZIs), facilitating the development of complex optical circuit designs.

Ongoing advancements in the design and fabrication of microring resonators contribute to their continuous improvement in performance characteristics. Researchers are enhancing the efficiency and efficacy of these resonators through refined development procedures, utilizing industrial deep ultraviolet (DUV) lithography and nanoimprint lithography techniques to improve precision and resolution. These advancements unlock the potential for creating novel and highly functional photonic devices, including logic gates, switches, lasers, and optical filters[45].

Incorporating reconfigurable wavelength routers into optical networks, particularly for point-to-point communication, holds promise for significantly augmenting transmission bandwidth. This development not only enhances current optical networking capabilities but also opens new research avenues, including on-chip sensors and biosensors. Despite these

advancements, challenges such as low processing tolerance, temperature sensitivity, and polarization dependence must be addressed to ensure the reliability, stability, and efficiency of microring based systems.

To achieve stability in microring resonators, temperature-controlled modules and advanced fabrication techniques are necessary to maintain performance over time. The introduction of polarization converters and splitters ensures polarization independence, allowing consistent operation regardless of the polarization state of the incident light. In integrated photonics, microring resonators play a pivotal and adaptable role, significantly impacting optical interconnectivity, optical computing, and communication systems. Their widespread adoption as fundamental building blocks for various optical devices, including filters, modulators, switches, logic gates, delay lines, and sensors[35], underscores their versatility and importance.

Various modification techniques can further enhance the functionality and versatility of microring resonators. By manipulating structural parameters or combining multiple resonators in unique configurations, a broad range of design possibilities emerges, enabling the creation of tailored optical devices. This flexibility positions microring resonators as indispensable tools for advancing optical device engineering and realizing sophisticated photonic systems. The typical configuration of a microring resonator involves its integration with a bus waveguide, resulting in straightforward arrangements with input and output ports. When the waveguide supports a single mode, the coupling region exhibits minimal loss, and polarization conversion is absent, allowing accurate quantification of optical losses within the microring resonator[35].

Microring resonators exhibit various architectural configurations, each characterized by different numbers of ports. This versatility enables the design of advanced photonic systems operating in various modes and port configurations. For example, add drop configurations allow selective wavelength filtering, while through port configurations enable seamless signal routing. Cross port configurations facilitate efficient signal splitting or combining, supporting tasks such as power distribution or signal duplication. Specific microring resonator configurations include a microring resonator coupled to a two-port bus waveguide and a microring resonator coupled to two four-port bus waveguides. These configurations are defined by parameters such as the coupling coefficient (k), ring radius (r), attenuation factor (α), transmitting coefficient (t), and optical field amplitudes (Et1, Et2, Ei1, and Ei2)[35]. These adaptable variations serve as fundamental building blocks, empowering researchers and engineers to develop customized photonic solutions tailored to specific requirements. Leveraging the inherent adaptability and flexibility of microring resonators enables the creation of novel architectural designs and advanced optical systems, driving progress in integrated photonics.

4.9. Photodetectors

Photodetectors are essential components in optical communication systems, serving as the interface between optical signals and electronic processing units. They detect light and convert it into an electrical signal, enabling the interpretation and processing of optical information. Photodetectors operate based on principles such as the photoelectric effect, where photons striking a semiconductor material generate electron–hole pairs that create a measurable current. Common types include photodiodes, avalanche photodiodes (APDs), and phototransistors. Photodiodes are valued for their simplicity and linear response, while APDs offer higher sensitivity and gain, making them suitable for low light applications. Performance is characterized by quantum efficiency, which measures the effectiveness of light to electrical signal conversion; response time, indicating how quickly a photodetector can follow changes in the light signal; and noise characteristics, affecting the signal to noise ratio. Advanced photodetector technologies, particularly those integrated into silicon photonics platforms, are continuously evolving to meet the demands of high-speed data transmission and high-resolution imaging, focusing on improving sensitivity, reducing noise, and enhancing integration with other photonic components.

4.10. PIN photodiodes

PIN photodiodes are characterized by their three-layer structure: a p-type layer, an intrinsic (i) layer, and an n-type layer, creating a high-resistance region between the p and n layers. This intrinsic layer is crucial for high sensitivity and fast response times. When light photons are absorbed by the intrinsic layer, they generate electron–hole pairs, which are then separated by the electric field across the p–i–n junction, resulting in a photocurrent proportional to the incident light intensity. PIN photodiodes are valued for their wide spectral response range, low noise characteristics, and high-speed performance, making them suitable for optical communication systems, medical imaging, and scientific research. Their performance is influenced by factors such as the width of the intrinsic layer, material properties, and the quality of the junctions. Recent advancements focus on improving quantum efficiency and reducing dark current to enhance sensitivity and signal to noise ratio.

4.11. Avalanche photodiodes (APDs)

Avalanche photodiodes (APDs) utilize avalanche multiplication to achieve high sensitivity and gain. APDs consist of a p–n junction operated under high reverse-bias conditions, creating a strong electric field that accelerates photo-generated carriers. When photons strike the APD, they generate electron–hole pairs that are accelerated by the electric field, gaining enough energy to ionize additional atoms, leading to a cascade of further electron–hole pair generations. This avalanche effect results in an amplified current proportional to the incident optical signal, advantageous for detecting weak light signals. APDs are particularly useful in low-light conditions and high-speed optical communication systems due to their high gain and low noise characteristics. They require precise biasing and temperature control to manage the avalanche process and maintain performance stability. Recent developments aim to enhance the gain-bandwidth product, reduce noise, and integrate APDs with advanced photonic circuits for improved functionality in various optical applications.

4.12. Function in converting optical signals to electrical

The conversion of optical signals to electrical signals is fundamental in optical communication systems, enabling informa-

tion transmission over optical fibers to be interpreted by electronic devices. This process is achieved using photodetectors, which absorb incident photons and generate corresponding electrical signals. In PIN photodiodes, the intrinsic layer's electric field separates the charges created by the photoelectric effect, generating a current proportional to the incident light intensity. In contrast, avalanche photodiodes amplify the photocurrent through impact ionization, providing higher sensitivity for detecting low-light signals. The electrical signal is processed by electronic circuits to reconstruct the original optical data, facilitating its use in data communication, imaging systems, and sensor technologies. The efficiency and accuracy of this conversion process are crucial for high-performance optical communication systems and the reliability of transmitted information.

4.13. Optical amplifiers

Optical amplifiers are crucial in optical communication systems for boosting the strength of optical signals without electronic conversion. They use a gain medium to amplify the signal through stimulated emission of radiation. Common types include erbium-doped fiber amplifiers (EDFAs) and semiconductor optical amplifiers (SOAs). EDFAs use a fiber doped with erbium ions, which, when pumped by a laser, provide gain to signals traveling through the fiber by stimulating the emission of additional photons. SOAs use a semiconductor material where electrical current creates a population inversion, leading to optical gain. The performance of optical amplifiers is characterized by gain, noise figure, and bandwidth, where gain represents the amplification level, noise figure indicates additional noise introduced by the amplifier, and bandwidth determines the operational wavelength range. Advances in optical amplifier technology focus on increasing gain, extending bandwidth, and minimizing noise to support high-speed, long-distance optical communication systems and improve fiber-optic network performance.

4.14. Semiconductor optical amplifiers (SOAs)

Semiconductor optical amplifiers (SOAs) amplify optical signals using semiconductor materials based on stimulated emission. An electrical current excites electrons in a semiconductor, creating a population inversion that allows the material to amplify incoming optical signals through stimulated emission of photons, increasing their intensity. SOAs are valued for their compact size, integration capabilities, and broadband amplification across various wavelengths, making them suitable for optical networks, signal processing, and WDM systems. Despite their advantages, SOAs can exhibit nonlinearities, gain saturation, and noise, which impact signal quality. Recent research focuses on optimizing material compositions, designing advanced structures, and integrating SOAs with other photonic components to enhance gain, reduce noise, and extend operational bandwidth.

4.15. Erbium-doped fiber amplifiers (EDFAs)

Erbium-doped fiber amplifiers (EDFAs) are pivotal in modern optical communication systems, providing high-gain amplification over long distances in optical fibers. They operate by doping a fiber optic core with erbium ions, which amplify optical signals through stimulated emission when excited by a laser pump source. Erbium ions release energy in the form of photons, amplifying the signal traveling through the fiber. EDFAs are particularly effective in the 1550 nm wavelength range, ideal for long-haul communication due to its low attenuation and dispersion. They offer high gain, wide bandwidth, and low noise figure, making them essential for extending the reach and capacity of optical networks. However, their performance can be influenced by pump power, fiber length, and other optical components. Ongoing research aims to improve EDFAs by enhancing efficiency, increasing gain, and reducing noise to support higher data rates and longer transmission distances in advanced optical communication systems.

4.16. Purpose in boosting signal strength

The primary purpose of optical amplifiers, such as semiconductor optical amplifiers (SOAs) and erbium-doped fiber amplifiers (EDFAs), is to boost the strength of optical signals in communication systems, enabling data transmission over long distances with minimal degradation. Optical amplifiers increase the intensity of optical signals without electronic conversion, maintaining data integrity and quality. They address signal attenuation and loss issues that occur as light travels through optical fibers, overcoming distance limitations and supporting high-speed data transmission. Optical amplifiers are also crucial for advanced communication techniques such as WDM, which requires simultaneous amplification of multiple wavelengths. By providing high gain, broad bandwidth, and low noise amplification, optical amplifiers enhance the performance and capacity of optical communication systems, making them indispensable for modern telecommunications and data networking.

5. Optimizing routing solutions for enhanced design efficiency

Optical ONoC systems require efficient pathways for data transmission and reception, necessitating specialized routers to switch signals between source and destination. Unlike traditional NoC systems that use electrical wires or wireless methods, optical NoC utilize waveguides for data transmission. This shift has led to the development of new routing methods and router designs, with significant emphasis on optical NoC in recent research and industry efforts[46].

One major design challenge is addressing deadlocks that can disrupt data flow. Specialized optical routers, designed with predefined routing algorithms, offer a potential solution by eliminating the need for buffers and virtual channels, which are impractical in optical systems. Instead, these routers rely on advanced routing mechanisms to manage data flow and avoid blockage. The diverse implementations of optical router architectures make deterministic classification challenging, as these routers can serve various functions and applications.

Optical routers can be categorized into all optical and hybrid types. All optical routers, though less versatile, are useful in specific scenarios, while hybrid routers combine technologies to enhance performance in bandwidth, power efficiency, and scalability. Specialized optical routers often incorporate microring resonators, which help reduce space consumption by eliminating the need for full communication between ports. Given the variation in designs and standards, a chronological approach may be beneficial for tracking technological progress.

Comprehensive analysis of photonic router architectures for ONoC systems. The pursuit of efficient on-chip communication within ONoC systems has led to exploring various technologies. Optical routers offer advantages such as enhanced bandwidth, reduced latency, and improved scalability. This section provides a detailed analysis of different optical router architectures, focusing on their design features and impact on on-chip communication.

We will examine the fundamental principles, design considerations, and performance implications of various optical routers, based on documented achievements in the literature. As the demand for higher bandwidth and lower power consumption increases in manycore processors, optical networks on chip present a promising alternative. Optical routers are crucial in these systems, significantly affecting overall network performance. Different routers feature various topologies, with mesh topologies commonly used for their simplicity and regularity, and port configurations typically ranging from 4 to 7[16–18].

6. Categorization of optical routers

Optical routers can be classified based on application requirements, performance objectives, scalability, power consumption, and fabrication feasibility:

MRR-based routers: These routers are compact, compatible with VLSI fabrication techniques, and capable of high-quality factor resonators, offering integration and space efficiency.

MZI-based routers: MZI-based routers provide flexible routing configurations, low crosstalk, and the ability to implement complex functionalities, suitable for adaptable routing solutions.

Hybrid routers: Combining various technologies, hybrid routers aim to improve performance in bandwidth, power consumption, and scalability.

The choice of router type depends on specific research or application goals. Researchers evaluate router architectures based on metrics such as throughput, latency, power efficiency, scalability, and integration capabilities to select the most suitable option.

Additionally, the reviewed works vary in detail regarding methods and results. Some studies provide comprehensive analyses and thorough reporting, while others are less detailed. This variability highlights the need for a balanced approach in evaluating and reporting research outcomes to advance optical router technologies.

6.1. Photonic router architectures: design principles, components, and performance

This section examines three primary types of optical routers: micro ring resonator (MRR) based, MZI-based, and hybrid architectures. By exploring the strengths and limitations of each design, we aim to gain a comprehensive understanding of the trade-offs associated with their implementation.

6.2. MRR-based optical routers

The paper "Microring resonator arrays for VLSI photonics" by Little *et al*. offers a thorough investigation into the analytical theory, fabrication, and potential applications of two dimensional (2D) microring resonator arrays[47]. The paper presents a theoretical framework for analyzing the scattering response of these arrays, which supports flexible interconnections among four port, single polarization nodes. It introduces a foundational architecture for optical routers based on microring resonators (MRRs), marking one of the initial efforts in this field, and utilizes a glass platform for implementation.

The analytical theory provides a detailed description of the scattering response of 2D microring resonator arrays, enabling the connection of multiple four port, single polarization nodes. To validate this theoretical model experimentally, the researchers fabricated an 8×8 cross grid array of vertically coupled glass microring resonators. The array consists of rings with a nominal radius of 10 μm, a core refractive index of 1.6532, and a cladding index of 1.4508. The ring waveguide heights are 1.5 μm, with widths ranging from 1.0 to 1.7 μm along upward directed diagonals to ensure uniformity. The spacing between parallel bus waveguides is 250 μm.

Transmission measurements were conducted on the fabricated array to assess the cross connect response of the upper left corner ring (input 1/output 1) and signal propagation along two sides of the array (input 2 to output 2). These measurements involved traversing sixteen junctions and interacting with fourteen additional rings. Results showed signal attenuation due to junction scattering loss and partial extraction by neighboring rings. Experimental estimations indicated a per-junction power scattering loss of 15%, attributed to imperfections in the junctions, which had rounded and flared corners. In contrast, theoretical simulations using the finite difference time domain (FDTD) method predicted a lower scattering loss of 1% per junction. The qualitative agreement between the theoretical predictions and experimental data supports the validity of the proposed theoretical model. Fig. 4 shows the 8×8 grid of microring resonators of this work.

The paper[48], investigates the potential applications of microring resonator arrays, highlighting their suitability for optical channel dropping filters, wavelength trimming, optical switching, and optical logic. These arrays offer several advantages, including compactness, scalability, low power consumption, and compatibility with VLSI fabrication techniques, making them promising candidates for on-chip communication systems.

The paper titled "on the design of a photonic network-on-chip" introduces a novel architecture for a photonic NoC that leverages the unique capabilities of optical technologies for on-chip communication[48]. It discusses recent advancements in nanoscale silicon photonic integrated circuitry that are compatible with CMOS fabrication, providing new opportunities for integrating optical technologies into the on-chip communications infrastructure.

The paper presents a detailed exploration of the proposed photonic NoC architecture, including its design, implementation, and evaluation through simulations. The architecture features a mesh topology with 16 nodes, each comprising a processor core, a cache, and a network interface. The network interface integrates photonic transmitters and receivers for optical signal communication, along with an electronic controller for managing packet routing and flow control. Key photonic network components, such as switches, modulators, and detectors, are seamlessly integrated with the electronic control network to ensure efficient and reliable data transmis-

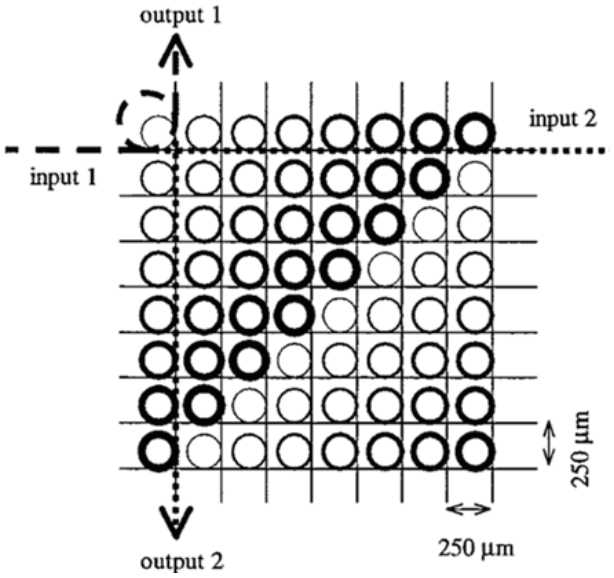

Fig. 4. Schematic diagram of an 8 × 8 array of microring resonators. Rings with the same waveguide width are drawn with the same point size[47].

sion.

The design includes a 4-port router equipped with 8 microring resonators, 4 waveguides, and 4 crossing waveguides, addressing fundamental network design challenges in chip multiprocessor (CMP) systems. Strategies are presented to address a blocking issue that negatively impacted the work, with simulations demonstrating the effectiveness of the proposed approach in resolving deadlocks.

Extensive simulations reveal that the photonic NoC achieves a throughput of 1.6 Tb/s, a latency of 2.5 ns, and a power consumption of 0.16 W, showcasing significant improvements over state-of-the-art electrical NoC architectures. The photonic NoC offers several advantages, including high bandwidth, low latency, and low power consumption. It supports multiple wavelengths and WDM to enhance network capacity and exhibits scalability and adaptability to varying traffic patterns and workloads.

An event driven simulator was developed to evaluate the architecture and conduct a series of investigations, demonstrating that low latency, low power photonic links can be established in tens of nanoseconds. The paper emphasizes the critical impact of optimizing the physical layer configuration of photonic components on network performance.

Despite its advantages, the paper acknowledges several challenges associated with the photonic NoC, such as the complexity of fabricating and integrating optical components with electronic circuits, high insertion loss and crosstalk in optical switches and links, limited buffering and processing capabilities in the network interface, and sensitivity to temperature variations and alignment errors in optical devices.

In summary, the paper provides a comprehensive exploration of a photonic NoC architecture, detailing its design, implementation, and simulation-based evaluation. The results highlight its superior performance in communication efficiency and scalability, offering high-bandwidth, low-latency, and low-power communication for chip multiprocessor systems. Despite the challenges, the photonic NoC represents a promising direction for future on-chip communication networks.

The paper titled "photonic noc for DMA communications in chip multiprocessors" details the development and application of a non-blocking photonic switch within a photonic NoC designed for efficient direct memory access (DMA) communications in chip multiprocessors[49]. The authors propose a folded torus topology for the photonic NoC to address latency and performance challenges associated with establishing photonic paths. The introduction of non-blocking photonic switches improves upon previous blocking switches, leading to enhanced performance, better utilization, and simplified injection and ejection switch structures. These innovations contribute to reduced latency and increased effective bandwidth by accounting for realistic optical losses and spatial requirements.

The paper assesses the optical loss budget and area requirements for the network implementation utilizing the new non-blocking photonic switches. Simulations demonstrate that this approach significantly reduces latency and enhances performance by increasing effective bandwidth. The authors also investigate integrating the direct memory access (DMA) communication paradigm within the photonic NoC, optimizing DMA block size to further enhance data transfer efficiency.

The advantages of employing a photonic NoC for DMA communications in chip multiprocessors include improved DMA performance, high bandwidth, low latency, and scalability. Photonic technologies facilitate high speed data transfers between memory and processing units, surpassing traditional electrical interconnects. The photonic NoC architecture supports scalability to accommodate increasing core counts, enabling the integration of multiple processing units.

However, challenges exist, such as the complex fabrication and integration of optical components with electronic circuits, which may require specialized techniques and incur higher costs. Additionally, the photonic NoC is sensitive to environmental factors like temperature variations and alignment errors, necessitating careful calibration and maintenance.

The design of the photonic switches for the folded torus topology includes injection switches, ejection switches, and routing switches. Injection switches, facilitating the entry of data packets into the network, are designed to minimize optical losses and reduce switch footprints by simplifying functionality and eliminating some waveguides and microrings. Ejection switches, located on the torus columns, forward data packets to gateway switches for network exit while minimizing optical losses and conserving space and power. Routing switches, central to the photonic NoC, manage data packet routing within the network with minimal latency, incorporating waveguides and microrings for dynamic routing. Although these switches have slightly larger footprints, their design ensures efficient data routing. Fig. 5 shows layout of the proposed components.

Overall, the photonic switch design aims to achieve high performance and reduced optical losses within the NoC. The compact, simplified structures of the injection and ejection switches contribute to lower power consumption and improved efficiency, while the larger routing switches provide essential functionality for seamless data routing. Integrat-

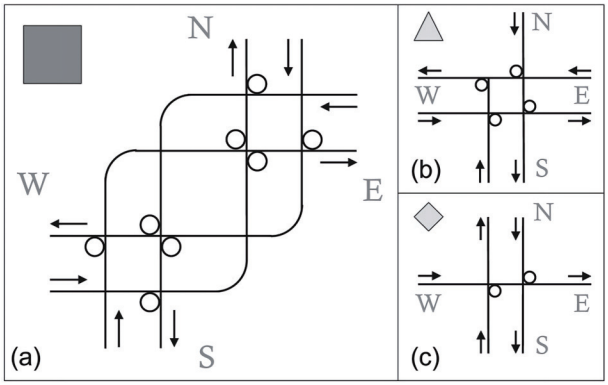

Fig. 5. Photonic component layout for (a) routing, (b) injection, and (c) ejection switches[49].

ing these photonic switches into the folded torus topology offers a scalable, low latency, and high bandwidth solution for DMA communications in chip multiprocessors. The estimated optical losses and area requirements are within the capabilities of current optical transceivers, highlighting the potential of photonic switches to enhance performance and reduce contention in chip multiprocessor systems.

In the paper titled "a compact and low power consumption optical switch based on microrings", the authors propose an innovative switch design utilizing microring resonators to construct an 8×8 matrix switch[50]. The paper introduces a notable optical switch matrix measuring 8×4, incorporating ring resonators with eight input channels and four pairs of add drop ports. This matrix switch features a non-blocking architecture and a cascade arrangement, comprising 192 switches organized into 64 triplets.

The authors also present two optical routers: the "direct router" and the "symmetric router". Both routers have four non-blocking ports and aim to reduce insertion loss while enhancing overall performance. Of particular interest is the "symmetric router", which leverages eight micro ring resonators, four waveguides, and eight waveguide crossings to optimize functionality.

The focus of the paper is on developing a compact and energy efficient optical switch based on microrings. The proposed design addresses the limitations of conventional optical switches, such as their large physical footprint and high power consumption. By harnessing the unique properties of microrings, the authors aim to provide a more compact and low power solution. key characteristics highlighted include the "compact design" and "low power consumption". The authors emphasize reducing the physical footprint compared to traditional switches and minimizing power requirements.

It is important to note that the paper does not cover other characteristics typically associated with routers in optical NoC systems, such as latency, bandwidth, scalability, integration with network topologies, performance metrics, control mechanisms, fault tolerance, or specific comparisons with other router designs.

The paper titled "a novel optical mesh network-on-chip for gigascale systems-on-chip" addresses the challenges faced by electronic NoC designs in nanoscale CMOS technologies, including energy consumption, bandwidth limitations, and latency issues[51]. With rapid advancements in nanoscale

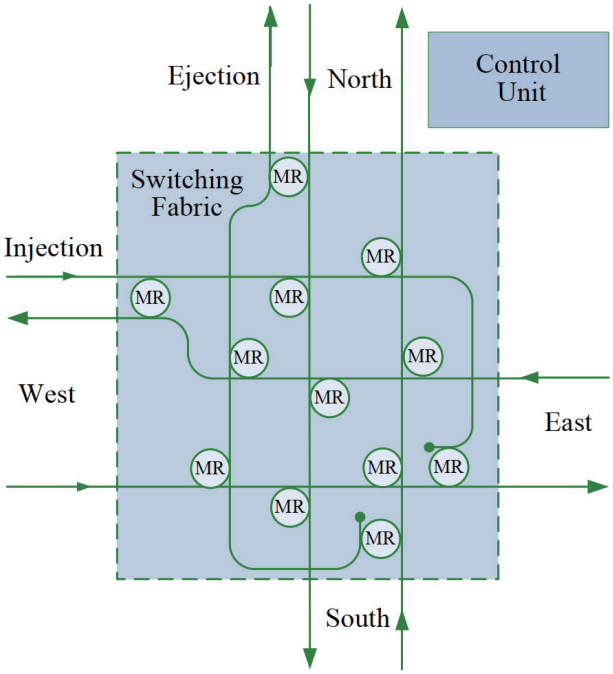

Fig. 6. (Color online) OXY architecture[51].

photonic technology, optical NoC (ONoC) have emerged as a promising solution to these problems. This study introduces a new non-blocking optical router, named OXY, and utilizes it to construct a 2D mesh ONoC. The OXY based optical mesh NoC benefits from XY routing features in 2D networks, significantly reducing the number of microring resonators required. The OXY architecture is depicted in Fig. 6.

To evaluate the proposed ONoC's performance, simulations were conducted using the OPNET network simulator, focusing on end-to-end (ETE) delay and throughput. ETE delay is defined as the average time from packet generation by processors to packet arrival at their destinations, encompassing both connection oriented path setup time and optical packet transmission time. Throughput is normalized under a given offered load. Simulations were carried out for mesh sizes of 6×6, 9×9, and 12×12.

The results indicate that larger networks experience more significant performance degradation. For instance, the 12×12 mesh saturates at a load of 0.1, while the 6×6 mesh reaches saturation at a load of 0.24. This discrepancy is attributed to the larger network generating more packets within a given timeframe, resulting in a higher load and an earlier saturation point.

Additionally, the OXY-based optical mesh NoC was compared with three alternative methods regarding microring resonators, loss, and energy consumption. The comparison demonstrated that the OXY based approach excels, with the lowest power consumption, minimal losses, and smallest area requirement. Notably, the OXY router maintains a small constant maximum power for routing packets, regardless of network size, and its maximum power consumption closely aligns with average power consumption.

The mesh ONoC constructed using the OXY router, consists of two interconnected networks: an optical network for handling large payload packets and an electronic network for control packets and small payload packets. Payload packets carry data and processor instructions, while control packets

convey network control information. The electronic network mirrors the optical network's topology, connecting the control units of all OXY routers.

The paper titled "cascaded active silicon microresonator array cross connect circuits for WDM networks-on-chip" introduces a novel optical switch concept on a silicon chip. This switch employs a 5 × 5 array of cascaded waveguide crossing coupled microring resonator based switches designed for photonic NoC applications[52]. To reduce loss and crosstalk, the authors use a multimode interference (MMI) based wire waveguide crossing design, which is more effective than traditional plain waveguide crossings. They incorporate a lateral p–i–n diode with the microring resonator to enable high speed on off switching at GHz frequencies through carrier injection mechanisms. The study assumes that all 25 microring resonators are identical within a relatively broad resonance linewidth.

The optical circuit switch can operate with either a single wavelength channel or multiple wavelength channels, spaced according to the microring resonator's free spectral range. The authors assess the potential performance of the proposed photonic network by analyzing the loss budget of light path cross connections and the DC on off power consumption needed to establish a light path. Initial experiments demonstrate 3.6 Gbit/s non return to zero data transmissions at on and off resonance wavelengths using cascaded passive silicon MMI crossing coupled microring resonators. However, the switch node design has limitations, including a relatively large footprint and substantial optical power loss introduced by the crossing array. Despite the MMI design's attempt to mitigate crossing insertion loss, simulations show a notable 0.1 dB insertion loss at each crossing, which poses a significant challenge to the optical power budget of a large scale mesh intra chip network. The 2D photonic is depicted in Fig. 7.

The proposed switch node is compatible with wavelength division multiplexing (WDM) technology. By splitting the photonic message into different wavelength channels separated by the microring resonator's free spectral range, the switch can simultaneously filter and transmit multiple wavelength channels. This approach, similar to fiber optic networks, provides an aggregated ultra high bandwidth interconnect for the NoC. Implementing WDM technology requires multiple laser sources or a spectrally sliced broadband light source precisely aligned with the microring resonances.

The design of the 5 × 5 nonblocking switch node comprises a 5 × 5 array of cross connected identical microring resonators operating at the same wavelength channel. This nonblocking switch node can be controlled by a simple routing algorithm, facilitating arbitrary one-to-one interconnections between any of the five input ports and any of the five output ports without contention. The input ports in the four directions are labeled Iwest, Ieast, Inorth, and Isouth, while the corresponding output ports are labeled Owest, Oeast, Onorth, and Osouth. Icenter and Ocenter denote local connecting ports for the core, which connects to a modulator and a receiver as the electrical–optical (EO) interface.

The paper[53], titled "development of a cascaded microresonator based matrix switch for silicon on-chip optical interconnection", examines the design and performance of a 5 × 5 matrix switch utilizing cascaded microresonator based electrooptic switches integrated with a waveguide cross grid on a silicon chip. This switch design features microring resonators arranged in a two-dimensional cascade, connected through multimode interference-based waveguide crossings to minimize loss and crosstalk.

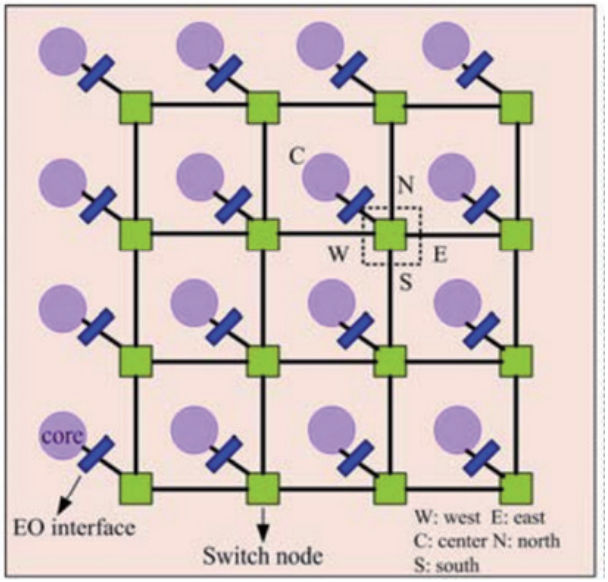

Fig. 7. (Color online) A 2D photonic mesh network-on-chip architecture is depicted[52].

The microresonator based matrix switch provides nonblocking interconnections among multiple input and output ports, offering benefits such as compact size, gigabit/second data transmission, nanosecond speed circuit switching, and low power consumption (approximately 100 μW per link). The design also supports potential large scale integration in NoC applications. An upgraded router design is introduced, adjusting for each port based on orientation, though the presence of numerous waveguide crossings poses scalability challenges for larger implementations.

The paper provides an extensive review of cascaded microresonator based matrix switches, emphasizing their advantages for silicon photonic interconnection networks in many core computing environments. It includes a detailed analysis of the microring resonator based cross grid switch design, assessing its capability for high data rate signal transmission and large scale integration. Proof of concept experiments demonstrate the switch's effectiveness in achieving fast switch times and high speed data transmission with minimal waveform distortion. However, issues such as optical power loss, resonance wavelength misalignments, and power consumption due to fabrication imperfections must be resolved for practical implementation. Fig. 8 illustrates the physical configuration of our proposed 5 × 5 photonic matrix switch, comprising 20 identical silicon microring resonator-based switch components connected to a 26-crossing MMI grid array.

The study includes a schematic and physical layout of the 5 × 5 matrix switch. The schematic features 20 microring resonator based switch elements connected to a multimode interference (MMI) crossing grid array with 25 crossings, illustrating light paths from five input ports to five output ports. The physical layout shows the switch's components, includ-

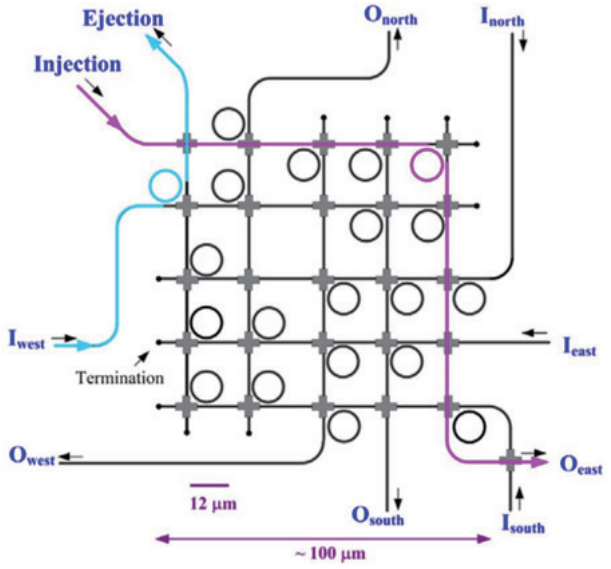

Fig. 8. (Color online) Physical configuration of our proposed 5 × 5 photonic matrix switch, which consists of 20 identical silicon microring resonator based switch components connected to a 26 crossing MMI crossing grid array[53].

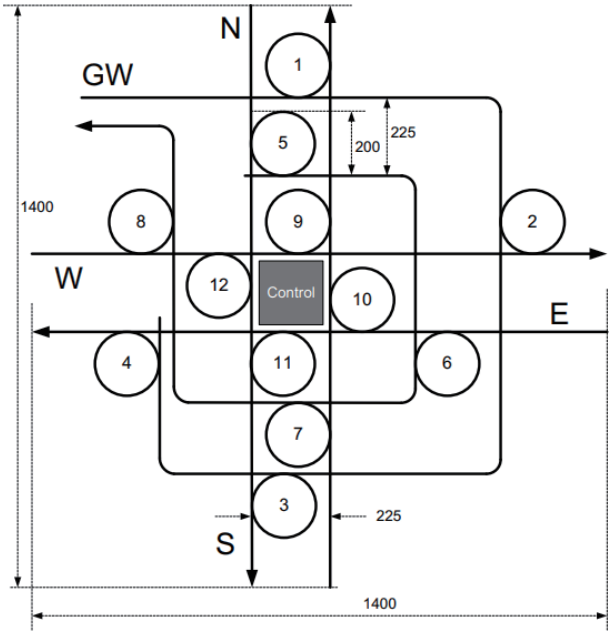

Fig. 9. Layout of photonic switch, showing waveguides and ring resonators[54].

ing an additional MMI crossing at the intersection of the Isouth and Oeast ports and termination points at unused ports.

The authors of Ref. [54] present a photonic NoC architecture designed to handle diverse communication demands in both time and space within arbitrary topologies. This architecture incorporates fairness principles to ensure high bandwidth optical circuits from end to end. Simulation results using scientific application traces indicate that the proposed architecture significantly outperforms both electrical and alternative photonic network topologies, providing 2–4 times the bandwidth at network saturation for random traffic and exhibiting an order of magnitude greater efficiency.

The photonic NoC features twelve micro ring resonators, six waveguides, and 19 waveguide crossings, forming a non-blocking router that facilitates efficient and seamless communication. In tests on a 64 core concentrated mesh, this technique demonstrated substantial improvements in network utilization. Under random traffic at network saturation, the proposed design achieved 2–4 times greater effective throughput compared to alternative designs, with energy efficiency improving by orders of magnitude over electrical counterparts.

Additionally, the time division multiplexing (TDM) arbitration mechanism used in the photonic circuit design proved at least four times more efficient for scientific application traces compared to a standard circuit switched photonic mesh. This underscores the adaptability and effectiveness of the proposed network design in real world scenarios, where efficient multi core communication is essential. The layout of the photonic switch, highlighting the waveguides and ring resonators illustrated in Fig. 9.

The photonic switch within the network includes waveguide paths and electro optically controlled photonic switching elements (PSEs) based on 200 μm ring resonators, which enable the spatial switching of wideband signals. The ports are labeled north, south, east, west, and gateway (GW). The optimization assumes X then Y routing, thus the switch does not require full connectivity between all ports. Signals traverse a ring only when originating from or destined for a gateway or when transitioning between dimensions. This design minimizes insertion loss for signals traveling in straight lines.

In a brief study[55], the authors designed and fabricated a bidirectional four port non-blocking optical router. This router features eight microring resonator based switching elements, four optical waveguides, and six waveguide crossings. Topology optimization was employed to minimize the number of waveguide intersections, thereby reducing crosstalk, transmission loss, and return loss associated with these crossings. The optimization also improved loss uniformity across various pathways in the optical router. Experimental results show that the through port achieves an extinction ratio of approximately 13 dB, while the drop port exceeds 30 dB. Crosstalk in the optical links is below −13 dB, indicating minimal interference. The router operates efficiently, with an average tuning power of about 10.37 mW and a tuning efficiency of 5.398 mW/nm. The functionality of the router and the preservation of optical signal integrity were validated through the successful transmission of a 12.5 Gb/s PRBS optical signal. MRR based bidirectional four port non-blocking optical router schematic is depicted in Fig. 10.

The router's design includes four waveguides, eight microring resonators (MRRs), and six waveguide crossings. A single ring coupled with two waveguides forms the fundamental building block of the proof of concept. the mrrs can be in an on or off state; the on state directs incident light into the mrr and towards the drop port, while the off state allows light to pass from the input port to the through port. all mrrs in the router have the same radius, enabling the support of both single wavelength channels and wavelength division multiplexing (WDM) signals with a channel spacing equal to the free spectral range (FSR) of the MRR.

The authors of Ref. [56] conducted experiments to demonstrate the implementation of non-blocking optical routers

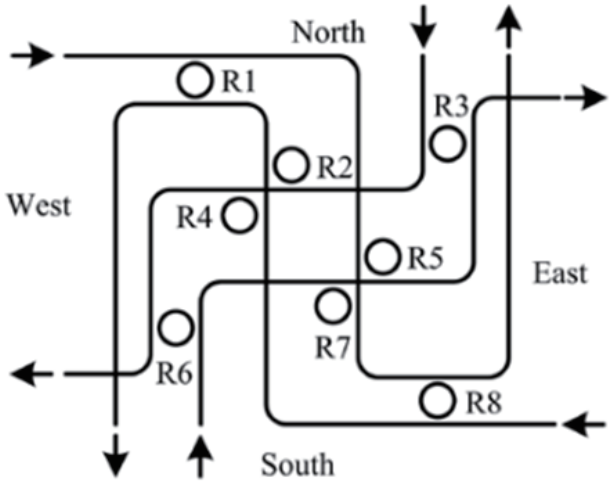

Fig. 10. MRR-based bidirectional four port non-blocking optical router schematic[55].

with four and five ports for photonic NoC. These routers use a cascade of microring resonators (MRRs) and feature a novel topology design aimed at enhancing performance metrics such as tuning power consumption, optical loss, crosstalk, and channel uniformity. The experimental setup included optical routers with four and five ports, where the four port router had a footprint of 300 × 340 μm^2 and the five port router measured 440 × 660 μm^2. Diagrams of five port non-blocking optical routers based on MRRs illustrated in Fig. 11.

Performance evaluation through static spectrum tests yielded notable results: the four port router exhibited a 3 dB bandwidth exceeding 0.12 nm, while the five port router surpassed 0.31 nm. The extinction ratios for the through ports were above 13 dB for the four port router and 20 dB for the five port router. For the drop ports, extinction ratios of 30 and 16 dB were achieved, respectively. High speed data transmission experiments using a 12.5 Gbps NRZ 231-1 PRBS pattern confirmed the routing functionality and signal integrity of the optical routers.

Overall, the study highlighted the significant advancements provided by the proposed four and five port non-blocking optical routers for photonic NoC. The innovative topology design resulted in reduced insertion loss, improved crosstalk, enhanced channel uniformity, and increased scalability compared to existing architectures. Fabricated on an SOI platform using a standard CMOS process, the optical routers were thoroughly characterized through static response spectra and high speed data transmission experiments, demonstrating their performance and functionality.

The routers employ cascaded microring resonators as their fundamental components. These MRRs exhibit two distinct states: on and off. In the off state, incident light with a wavelength of $\lambda 0$ from the input port bypasses the MRR and is directed towards the through port. In the ON state, light at $\lambda 0$ from the input port is coupled to the MRR and guided towards the drop port.

A technique for constructing a scaled non-blocking optical router is proposed in Ref. [57]. The authors present a universal method for building N port non-blocking optical routers using microring resonators. This approach is demonstrated through topologies for five, six, seven, and eight port routers. The simulations show that the five port optical routers offer a

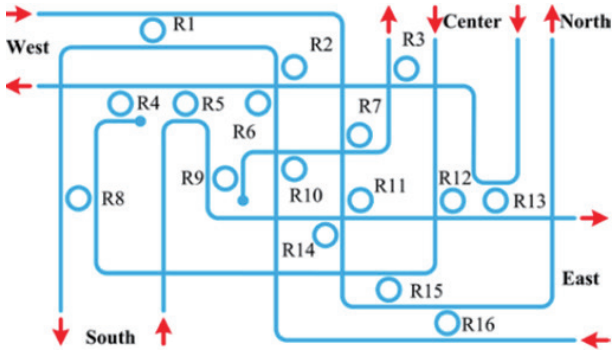

Fig. 11. (Color online) Diagrams of five port non-blocking optical routers based on MRRs[56].

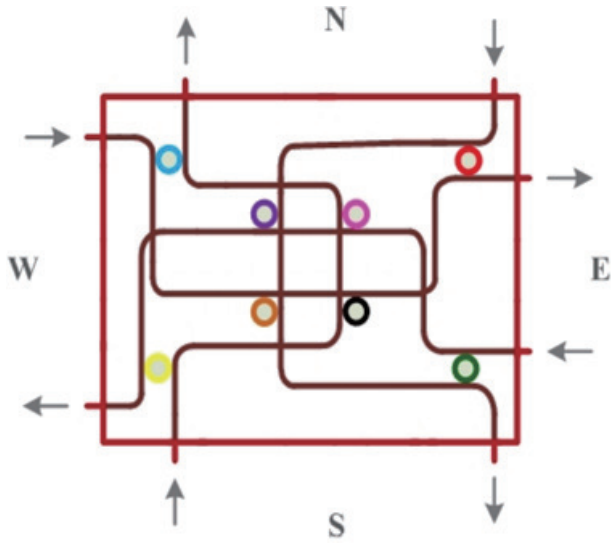

Fig. 12. (Color online) Helix-h switch configuration[58].

mesh photonic network with minimal insertion loss and a high optical signal to noise ratio (OSNR).

To build an N port non-blocking optical router, the method requires $n(n-1)$ microring resonators, $n(n-2)$ waveguide crossings, and n waveguides. Each optical path in the router's $n(n-1)$ optical router requires that a microring resonator be active at all times. The proposed technique simplifies the construction of high radix optical routers, enabling the implementation of more complex and efficient networks.

Comparative analysis shows that the five port non-blocking optical router built using this method has fewer microring resonators, waveguides, and average crossings per link, leading to reduced crosstalk, insertion loss, and power consumption. Modeling studies indicate that the 16 × 16 mesh network constructed with this optical router achieves the lowest average insertion loss and the highest worst case OSNR. The proposed method also supports the development of high radix non-blocking optical routers, facilitating advanced network architectures such as c mesh and Clos networks.

The construction approach reduces the number of waveguide crossings, waveguides, and microring resonators required, improving performance and scalability. The practical topology of the N port non-blocking optical router constructed with this method is significantly simpler than those shown in previous figures. The topologies for five, six, seven, and eight port non-blocking optical routers, as constructed using this method, are focused on the blue waveguide, with

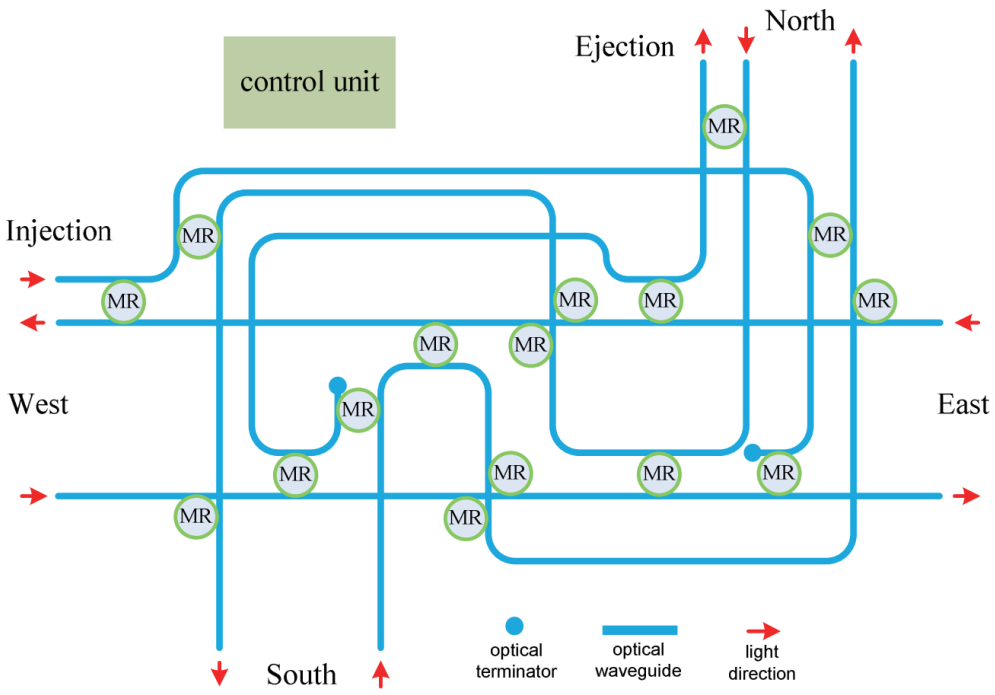

Fig. 13. (Color online) Architecture of Cygnus router[59].

green microring resonators (MRRs) representing drop points and yellow MRRs representing add points. Each constructed optical router exhibits central symmetry, adhering to the described rules.

To reduce power consumption, optical insertion loss, and the number of micro ring resonators (MRRs) and waveguide crossings, a recent design introduces a 44 non-blocking photonic router based on a micro ring resonator[58]. This innovative low insertion loss switch, called Helix-h, integrates a topology independent component to enhance physical layer and network performance metrics. By facilitating space routing in chip multiprocessor (CMP) networks, it reduces waveguide crossings and optimizes the use of additional wavelength channels. The Helix-h switch supports non-blocking connectivity for hundreds of on-chip cores while improving latency and energy efficiency. Evaluations using representative scientific applications suitable for CMP networks show significant performance improvements with the helix-h switch. In a mesh topology, it achieves a 112% increase in bandwidth compared to the previous highest performing switch design. Execution time and energy efficiency improve by up to 92% and 99%, respectively, for representative multicore applications. These enhancements underscore the Helix-h switch's effectiveness in improving system performance. The configuration of the Helix-H switch is depicted in Fig. 12.

Additionally, the use of unweighted directed graph features has enabled the development of generalized blocking recognition procedures for CMP interconnection network switches, providing a comprehensive understanding of blocking conditions in photonic switches. The Helix-h router's architecture includes 8 mrrs and 8 waveguide crossings, with 4 waveguides integrated into the system. These features contribute to the router's efficiency and performance in on-chip communication. Overall, the Helix-h switch demonstrates substantial improvements in bandwidth, execution time, and energy efficiency, making it a promising solution for high performance on-chip communication in multicore systems. The switch comprises eight 1 × 2 path selection elements (PSEs), including four parallel and four cross PSEs, along with four waveguides and eight waveguide crossings, enabling full connectivity between all ports and supporting various routing algorithms.

Cygnus, introduced in Ref. [59], is an optical router designed specifically for optical NoC. It operates in a strictly non-blocking manner and features a high performance, low power, and cost-effective architecture. Utilizing a 5 × 5 configuration based on silicon micro resonators, Cygnus offers significant advantages in power efficiency, signal integrity, and cost-effectiveness compared to traditional crossbar architectures.

Comprehensive comparative analysis shows that cygnus outperforms conventional crossbars in power consumption, signal loss, and micro resonator utilization. It achieves notable reductions of 50% in power consumption, 51% in signal loss, and 20% in micro resonator requirements. Specifically, Cygnus consumes only 3.8% of the power used by high-performance 45 nm electronic routers, resulting in an impressive 96% reduction in power consumption. Architecture of cygnus router is depicted in Fig. 13.

A key feature of cygnus is its passive routing capability, which ensures consistent low power consumption when using the dimension order routing algorithm, regardless of network size. This feature guarantees minimal and constant power requirements for packet routing. Additionally, both the maximum and average power usage of cygnus are closely aligned.

In comparison to other micro resonator-based routers, cygnus has been thoroughly evaluated in terms of power consumption, optical power insertion loss, and micro resonator utilization, demonstrating the lowest power consumption, signal losses, and micro resonator requirements among the evaluated routers.

Cygnus's architecture is strictly non-blocking and operates in a 5 × 5 configuration. It consists of a switching fabric

and a control unit that uses electrical signals to configure the switching fabric based on routing requirements. The switching fabric is constructed from two fundamental switching elements and incorporates 16 micro resonators, six waveguides, and two waveguide terminators. All micro resonators in the switching fabric are identical, with the same on state (λ_{on}) and off state (λ_{off}) resonance wavelengths. Cygnus operates using a single wavelength corresponding to λ_{on}. To reduce the number of micro resonators and save power, the final micro resonator on the waveguide for the injection port can be replaced with a Y-branch, although this modification introduces increased loss for packets exiting from the east port.

The non-blocking nature of Cygnus is demonstrated by examining all possible routing cases. In contrast, other optical routers typically use a conventional fully connected crossbar for their switching fabric. For an $N \times N$ optical router without U-turn support, an $N \times N$ crossbar configuration requires $N(N-1)$ micro resonators, $2N$ crossing waveguides, and $2N$ optical terminators.

The authors also developed a wavelength assignment scheme for GWORs with even and odd numbered input/output ports. In principle, an NN GWOR requires $N-1$ input wavelengths and $N(N-2)$ MRRs (for $N = 2n$) or $(N-1)2$ MRRs (for $N = 2n+1$) to enable routing.

The paper titled "a generic optical router design for photonic network-on-chips"[60] presents a scalable and non-blocking passive optical router called the generic wavelength routed optical router (GWOR), which utilizes micro ring resonator (MRR) technology. The authors introduce four 4×4 GWOR structures as foundational elements for constructing larger GWORs. This design minimizes the number of MRRs needed compared to existing passive router designs of equivalent network size and demonstrates reduced power loss. Basic 4×4 GWOR structures are illustrated in Fig. 14.

To improve bandwidth and fault tolerance, the authors propose the redundant GWOR (RGWOR) structure, which offers multiple routing paths between each input output pair. They also devise a wavelength assignment scheme for GWORs with even and odd numbered input/output ports. Specifically, an $N \times N$ GWOR requires $N-1$ input wavelengths and $N(N-2)$ MRRs for $N = 2n$ or $(N-1)2$ MRRs for $N = 2n+1$ to enable routing. The GWOR design effectively reduces the MRR count and power loss for light signals compared to prior non-blocking router designs. Being passive, GWORs do not need the power consuming TO/EO tuning and control circuits required by active optical routers.

The authors suggest that the GWOR design is suitable for high performance, low power photonic NoC systems. They also propose a redundant GWOR structure achieved by cascading basic GWORs at different levels to provide multiple routing pathways between any given input output pair. The paper highlights the GWOR design's benefits, including reduced power loss, minimal MRR usage, and its potential for high performance photonic NoC systems.

The extended portions of vertical waveguides and newly added waveguides are highlighted in blue, showing the general construction process of Type Ⅰ GWOR from another Type Ⅰ GWOR. The intersections of any two groups of waveguides form a single primitive 4×4 GWOR, with each pair of orthogonal waveguides having a unique intersection point.

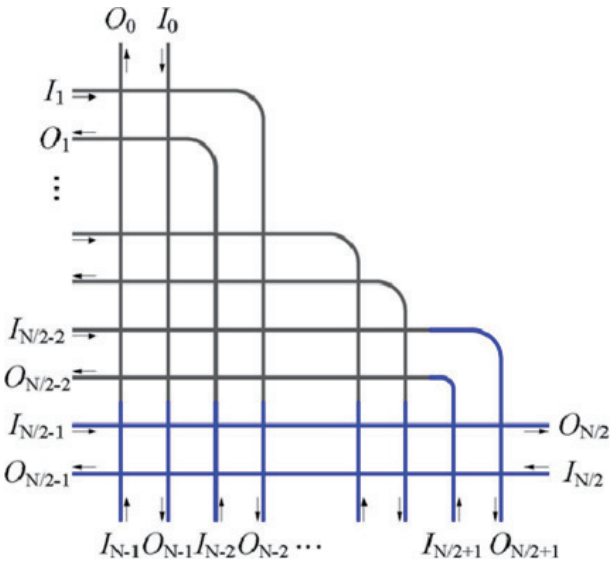

Fig. 14. (Color online) Basic GWOR structures[60].

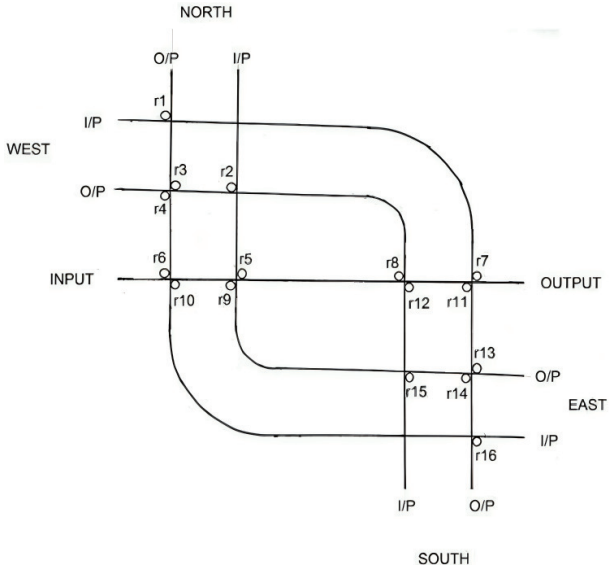

Fig. 15. Five port non-blocking optical router[61].

The four types of 4×4 GWORs introduced–Type Ⅰ, Type Ⅱ, Type Ⅲ, and Type Ⅳ–serve as the building blocks for designing larger and more functional GWORs, enabling scalable and flexible photonic NoC architectures.

The authors in Ref. [61], have proposed a routing scheme for a five-port optical router that utilizes sixteen microring resonators (MRRs), four bends, and fourteen crossings. The analysis indicates that the router benefits from reduced insertion losses due to the decreased number of crossings. The MRRs are controlled using the thermos-optic effect.

In their design, modeling, and analysis of the non-blocking MRR based silicon optical router, the authors employed the thermos-optic effect to tune the sixteen MRRs, twelve crossings, and four waveguide bends. Two key findings emerge from this study. Firstly, the symmetry of the router significantly affects its speed performance. Secondly, the number of crossings notably influences the optical losses during data transfer within the router's links. Specifically, reducing the number of crossings by two can decrease the overall optical loss by approximately 3.41%. Five port non-blocking optical router is shown in Fig. 15.

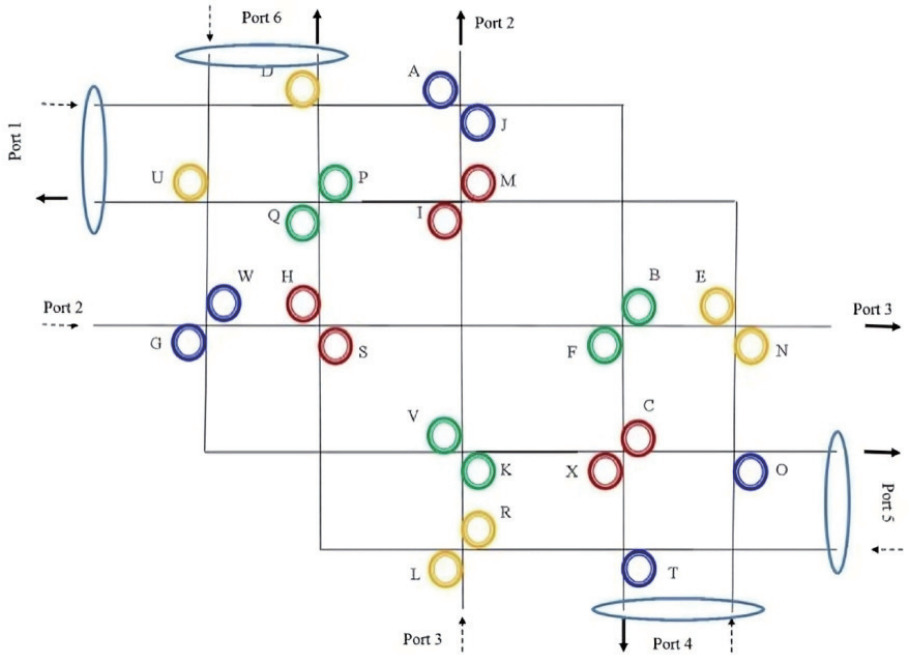

Fig. 16. (Color online) Diagram of 6 × 6 wavelength router topology[62].

The proposed optical router design demonstrates exceptional symmetry compared to other designs, resulting in reduced losses, enhanced switching speed, and lower power consumption. The design was simulated and implemented using the Phoenix software platform. The analysis of various parameters revealed that the proposed design is more efficient, with decreased insertion loss and power consumption. For the design parameters, the off-state throughput port transmission loss (Loff) was −0.3 dB, the on-state drop port transmission loss (Lon) was −0.86 dB, and the multimode interference (MMI) crossing loss (Lcross) was −0.18 dB.

Insertion losses were calculated for all links, with specific results for each link. For instance, the link from north to south, which included 5 crossings with 3 MRRs (1 MRR in the on state), had a calculated insertion loss of −2.66 dB. The study also found that while power consumption increased in 8 links, it decreased in 12 links, with no change observed in one link. The average power consumption for the previous design was 2.1753 dB, whereas it decreased to 2.1009 dB for the proposed router, representing a nearly 3.4% reduction in power consumption.

Overall, the simulation and implementation of the proposed design demonstrate its efficiency, marked by reduced insertion loss and power consumption compared to the previous design. The router architecture follows a 5 × 5 topology, allowing links in all four directions and a local processor. It incorporates 16 MRRs, 4 bends, and 14 crossings, with a layout that emphasizes symmetry and optimized MRR placement, yielding advantages such as high speed, a simplified switching matrix, and reduced losses. The careful arrangement of MRRs prevents signal blocking between microrings and within the router topology.

Ref. [62] details the development of a 6 × 6 router based on a photonic crystal ring resonator (PCRR). Fabricated using silicon pillars with air perforated structures, the router exhibits a refractive index of 3.47 and operates within the third optical window, which is favored for optical communication systems due to its minimal loss characteristics. The bandgap of the router is analyzed using finite difference time domain (FDTD) and planar expansion methodologies. The router demonstrates desirable performance attributes, including low crosstalk, minimal propagation delay, and low insertion loss.

The evaluation process via FDTD shows that the router achieves favorable benchmarks for crosstalk, insertion loss, and propagation delay. The maximum values for these parameters are determined for the structure. The routing path can be customized to meet specific application requirements. The router's compact footprint, measuring 4900 μm^2, makes it a promising candidate for future fully integrated optical circuits in the telecommunications industry. Fig. 16 shows the diagram of 6 × 6 wavelength router topology.

The 6 × 6 router, consisting of 24 densely arranged ring resonators, is designed to operate within the third optical window, known for its low attenuation loss. Routing of wavelengths between the six input and output ports is managed using four 1 × 2 and ten 2 × 2 routers. The routing elements and their corresponding wavelengths for all 30 pathways in the 6 × 6 wavelength router are detailed. To facilitate routing for four out of five wavelengths, the router employs 24 ring resonators (labeled A to X), while one wavelength does not require resonators for inter-port routing. Each ring resonator is tuned to specific resonant wavelengths to optimize transmission, with resonators organized into four sets of six, each with a designated resonant wavelength.

The authors in Ref. [63] present a novel 7 × 7 non-blocking optical router based on the dimension order routing (DOR) algorithm, aimed at optimizing the performance of optical NoC (ONoC) by minimizing the exposure of optical signals to MRRs and waveguide crossings, which are critical components in these networks. The proposed router design focuses on minimizing the number of MRRs involved, thereby reducing crosstalk and insertion loss across the network.

To evaluate the performance of the proposed optical

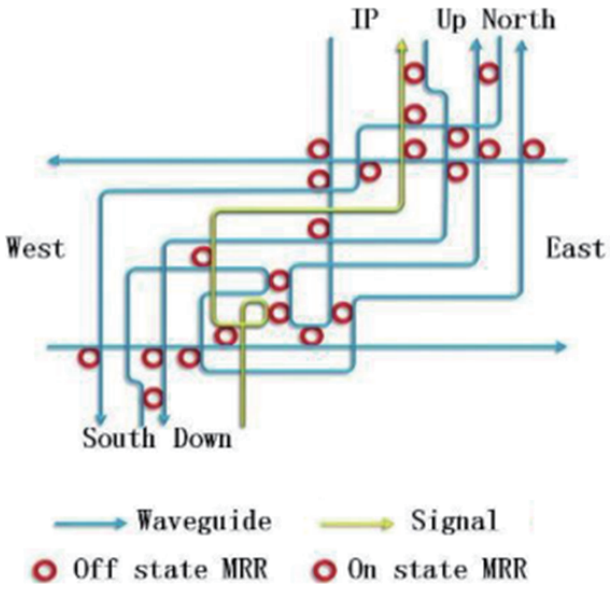

Fig. 17. (Color online) DORR router architecture[63].

router, comparisons were made with Ye's router and an optimized crossbar designed for a 3D Mesh network using the XYZ routing algorithm. Unlike many other studies, this work considers both router level and network level factors, offering a comprehensive assessment of the router's impact on overall network performance. DORR router architecture is depicted in Fig. 17.

The evaluation results demonstrate significant improvements with the proposed router. In terms of worst-case network insertion loss, it outperforms Ye's router, the optimized crossbar, the optimized universal OR, and the optimized VOTEX by approximately 8.7%, 46.39%, 39.3%, and 41.4%, respectively. This improvement underscores the router's effectiveness in reducing signal loss and maintaining signal integrity. Additionally, the proposed router shows substantial reductions in the worst-case optical signal to noise ratio (OSNR), achieving improvements of approximately 27.92%, 88%, 77%, and 69.6% compared to Ye's router, the optimized crossbar, the optimized universal OR, and the optimized VOTEX, respectively. These enhancements in OSNR contribute to better signal quality and reliability.

Furthermore, the power consumption of the proposed router is significantly lower than that of the other routers, with power savings of around 3.22%, 23.99%, 19.12%, and 20.18% compared to Ye's router, the optimized crossbar, the optimized universal OR, and the optimized VOTEX, respectively. This energy efficiency is crucial for reducing operational costs and promoting sustainable network design.

The authors also introduce the concept of the "least number of MRRs theorem", demonstrating that the proposed DOR based router achieves the minimum number of MRRs. This design not only improves performance metrics but also reduces waveguide crossings, leading to better area utilization and cost efficiency in the hardware implementation of the router.

Overall, the comprehensive evaluation and performance comparison underscore the effectiveness of the proposed optical router in reducing insertion loss, improving OSNR, and minimizing power consumption. The innovative design and optimization techniques make it a promising solution for 3D photonic NoC, offering improved performance and efficiency for future optical network architectures. By reducing the number of waveguides and establishing direct connections between ports, the design ensures that all ports can communicate directly with at least one other port, eliminating the need for additional MRR activation and thus saving energy and preventing an increase in the network's thermal state.

A five port, spatially non-blocking optical router based on microring resonators tuned via the thermos-optic effect is experimentally demonstrated in Ref. [64]. The router is fabricated on a silicon on insulator (SOI) platform using standard CMOS processing techniques, with microring resonators as its core components. These resonators are tuned through the thermos-optic effect to achieve balanced performance across the router's two output ports. The design ensures approximately symmetric performance in terms of insertion loss, extinction ratio, and crosstalk, making the router highly suitable for photonic NoC. The router is compact, with an effective footprint of 440 × 660 μm^2, and operates at a wavelength of 1551 nm. It exhibits an extinction ratio of over 21 dB for the through port and more than 16 dB for the drop port, with a 3 dB bandwidth exceeding 0.31 nm (38 GHz).

High speed signal transmission experiments at 12.5 Gbps were conducted to validate the router's routing capabilities. However, demonstrating an electro-optic tuning scheme for this device is challenging due to fabrication process tolerances. Despite this, the electro-optic switching scheme is anticipated to gain popularity in the future, as it allows for smaller, more compact structures with faster switching times and lower power consumption. Diagram of the five port non-blocking on-chip optical router is shown in Fig. 18.

The proposed five port optical router utilizes cascaded microring resonators (MRRs) and supports bidirectional communication across its center, east, south, west, and north ports. Control is achieved through an integrated electronic circuit on the same chip. The MRRs used in the router have uniform structural parameters and initial resonances, regardless of process nonuniformity, enabling efficient operation with both single wavelength and wavelength division multiplexing (WDM) signals. The router's non-blocking functionality is ensured by establishing dedicated physical links for each input output combination, resulting in 20 possible optical links, while prohibiting communication between the input and output of the same port. These links are formed using specific resonant MRRs or direct waveguide connections.

The router features 44 routing states, each involving five parallel input to output optical links. Unlike traditional metallic wires, optical waveguide crossings are used in photonic circuits, enabling complex routing within a two-dimensional (2D) layer. However, waveguide crossings introduce additional transmission loss, reflection loss, and crosstalk. To address this, the router's topology is designed to minimize the number of crossings. The five port optical router contains 16 MRRs and 14 crossings, resulting in reduced insertion loss, crosstalk, device area, and power consumption. By minimizing the number of crossings and MRRs, the router achieves improved device area utilization and power efficiency.

This paper discusses the development and experimental characterization of a highly integrated 8 × 8 optical router

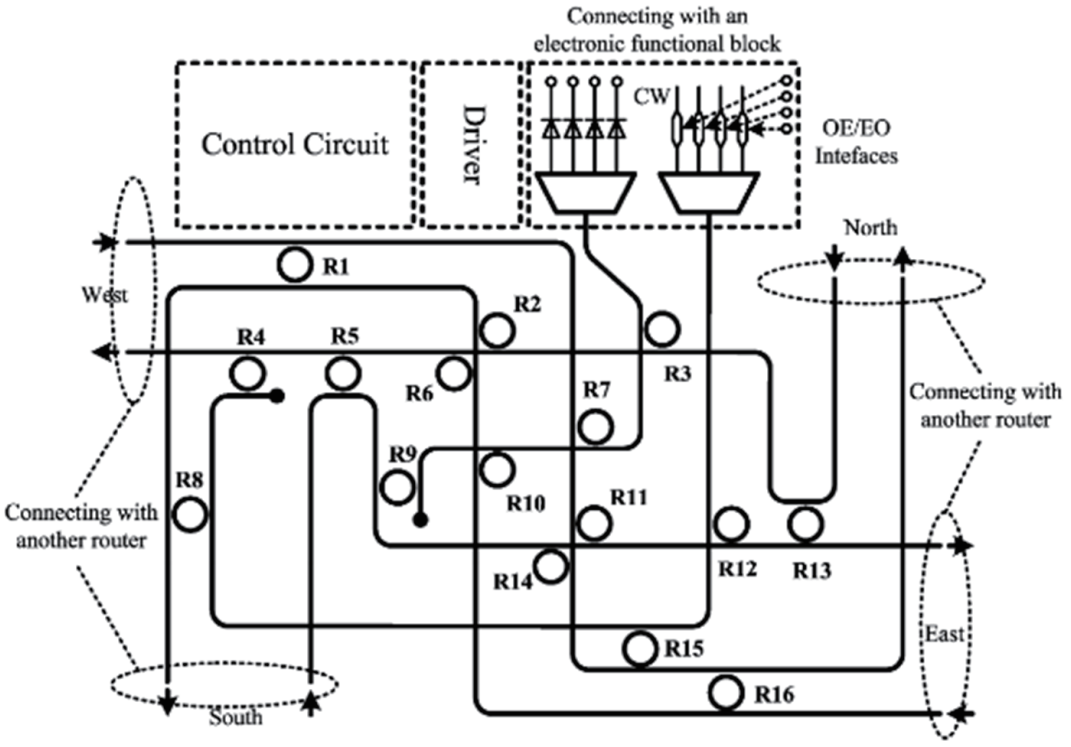

Fig. 18. Schematic layout of the five port non-blocking on-chip optical router[64].

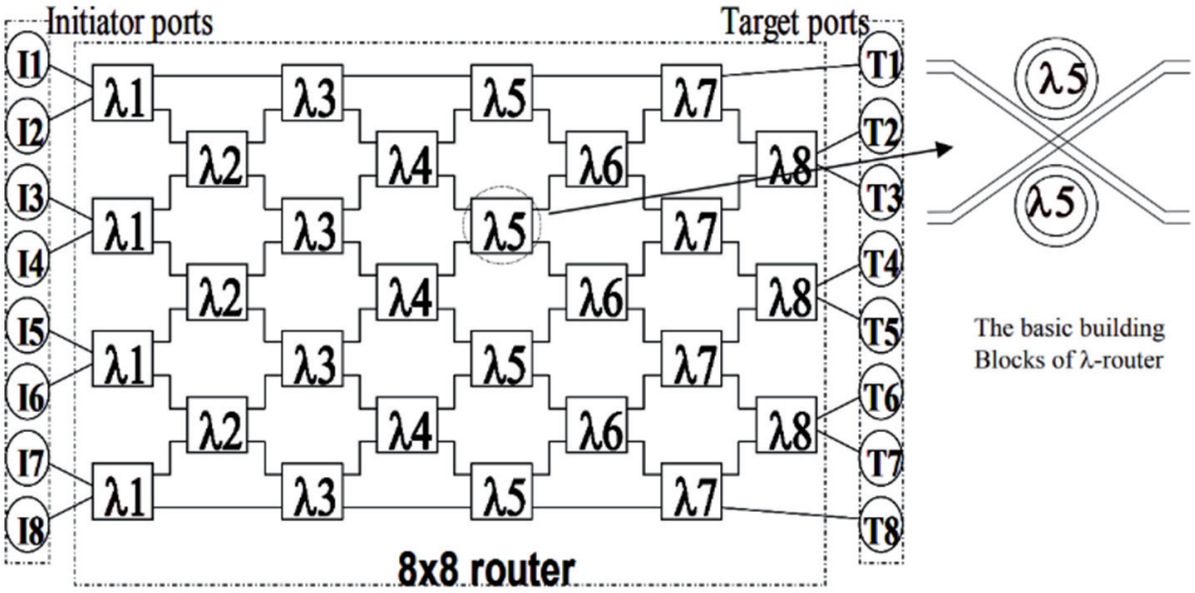

Fig. 19. 8 × 8 ONoC 8 x 8 architecture[65].

based on microring resonators with 2 × 2 multimode interference (MMI) crossings[66]. The router was fabricated using CMOS compatible silicon on insulator (SOI) technology, ensuring alignment with standard fabrication processes. The microring resonators in the router have a nominal radius of 2.5 μm, with slight variations of 10 nm, enabling a free spectral range (FSR) of 32 nm and a channel spacing of 4 nm. Experimental results closely match the modeled behavior, confirming the router's performance.

The fabricated router exhibits the following characteristics: the basic add drop filters in the device show losses of −2 dB and a resonance on/off contrast of 20 dB. Each channel in the router experiences an overall loss of approximately −4 dB, with a channel imbalance of less than 2 dB across the eight channels. Future research will focus on improving the router's performance by reducing the loss of the add drop filters. This includes exploring a new λ router design with a racetrack resonator to enhance signal drop performance and better control the coupling factor. Additionally, the study will work towards realizing a complete optical (ONoC) by using a wafer bonding process to integrate micro sources and photodetectors on top of the passive λ router.

Fig. 19 illustrates an 8 × 8 λ router configuration featuring initiator and target ports. In this configuration, each initiator port (I) and target port (T) comprises a group of 8 resonant micro ring sources and detectors that are coupled to a single Si strip waveguide. The data transmission within the passive λ router occurs optically, where a specific wavelength is

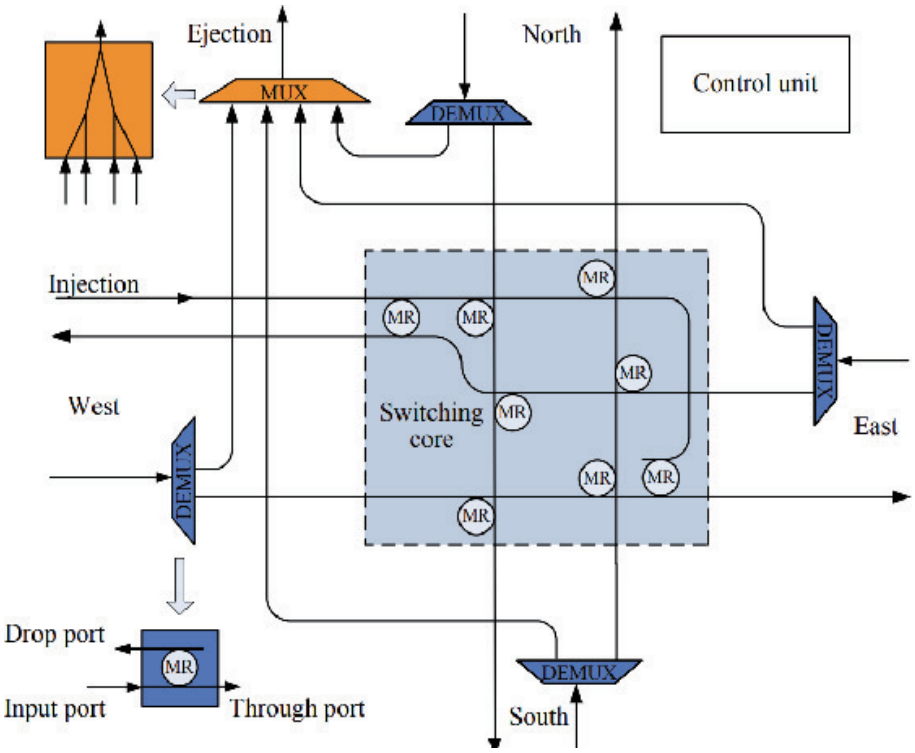

Fig. 20. (Color online) ODOR architecture[66].

chosen to send data from each initiator to one or multiple targets. Notably, a unique physical path exists between Ii and Tj for a given wavelength.

By integrating microring resonators with MMI crossings and leveraging CMOS compatible fabrication processes, this 8 × 8 optical router demonstrates significant potential for advanced photonic networks. Its compact design, precise control of channel spacing, and low losses make it a promising candidate for efficient, high performance optical communication systems. The 8 × 8 λ router configuration features initiator and target ports, with each port consisting of a group of eight resonant microring sources and detectors coupled to a single silicon strip waveguide. Data transmission within the passive λ router occurs optically, where a specific wavelength is selected to send data from each initiator to one or multiple targets. Importantly, a unique physical path exists between each initiator and target pair for a given wavelength.

The authors of Ref. [66], proposed a novel optical router architecture for optical networks-on-chip (NoC) called optical dimension order router (ODOR), which is based on the XY routing algorithm. They compared ODOR with four other router architectures and conducted a detailed analysis of three key factors: power consumption, optical power insertion loss, and the number of micro resonators. The results showed that ODOR required the fewest micro resonators, exhibited the lowest power consumption, and had the lowest insertion losses. Specifically, compared to a fully connected crossbar, ODOR consumed 40% less power, had 40% lower losses, and utilized 52% fewer micro resonators. Notably, ODOR maintains a small constant maximum power requirement for packet routing, regardless of network size. With current technology, the maximum power consumption is 0.96 fJ per bit, with the average and maximum power consumption being nearly identical.

The authors also demonstrated the end-to-end delay and network throughput of a 6 × 6 2D mesh NoC based on ODOR, using various offered loads and packet sizes typical of system-on-chip (SoC) applications. The simulation results highlighted the performance of ODOR and the XY routing algorithm in terms of end-to-end delay and network throughput within the proposed NoC architecture. The ODOR architecture is shown on Fig. 20.

ODOR's architecture includes a switching fabric and a control unit. The control unit uses electrical signals to configure the switching fabric according to the routing requirements of each packet. The switching fabric comprises input demultiplexers (DEMUXs), an ejection multiplexer (MUX), and a switching core. Both the input demultiplexers and the switching core employ identical micro resonators (MRs) with the same on state and off state resonance wavelengths, denoted as λ_{on} and λ_{off}. ODOR operates with a single wavelength corresponding to λ_{on}.

For each input port (East, North, West, and South), a demultiplexer is used, constructed with the fundamental 1 × 2 switching element in a parallel structure to avoid insertion loss from waveguide crossings. The demultiplexers separate packets destined for the current tile from those passing through the router. If a packet's destination is the current tile, it is directed to the ejection multiplexer without entering the switching core. If the destination lies outside the current tile, the packet is routed to the switching core and switched to one of the four directions. This separation scheme reduces the traffic entering the switching core and simplifies its complexity. Additionally, to minimize the worst-case accumulated insertion loss in the network, the drop ports of the 1 × 2 switching elements are connected to the ejection multiplexer, ensuring efficient routing and improved overall network performance.

This paper presents two novel designs for five port non-

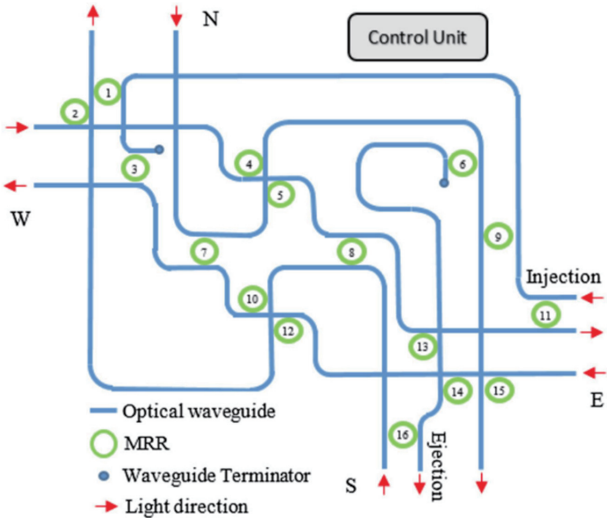

Fig. 21. (Color online) Architectures of the 5 × 5 non-blocking optical routers[67].

blocking ONoC routers, utilizing waveguides and microring resonators (MRRs) to minimize power losses and reduce the number of components[67]. The performance of these routers was evaluated in terms of power insertion loss and the required number of MRRs, comparing them to previously reported optical routers.

The first proposed design reduces average loss by 1.3% and maximum port-to-port loss by 9.8% compared to the cygnus router. Additionally, it achieves a 43% reduction in average loss and a 35 % reduction in maximum port-to-port loss when compared to traditional crossover router losses. The second design further optimizes performance, reducing average loss by 4.8% compared to the cygnus router. It also lowers average and worst-case losses by 46% and 35%, respectively, compared to a traditional crossbar router, while employing 6% fewer MRRs than the cygnus router. Architectures of the 5 × 5 non-blocking optical routers are shown in Fig. 21.

The findings indicate that the proposed designs allow for the miniaturization of ultra-high speed optical chips and are the most efficient in terms of requiring the fewest MRRs and exhibiting the lowest insertion loss. This makes the designs both more efficient and compact. The results also suggest that these optical routers can be effectively implemented in future three-dimensional multi core processors and WDM systems. The provided figures illustrate various optical router architectures for on-chip communication in ONoC systems, showcasing designs that ensure efficient, non-blocking communication.

In their study[68], the authors introduce a 6 × 6 optical router, Panzer, designed to meet the scalability requirements of network chips. Panzer demonstrates the lowest insertion loss and requires fewer microring resonators (MRs) compared to other router designs. Simulations were conducted on a 64-core enhanced mesh network built using Panzer, yielding results for end-to-end delay and network throughput under neighbor traffic patterns. These simulations highlight the effectiveness of the Panzer based mesh in managing various traffic scenarios. The authors plan to explore new topologies considering Panzer's characteristics, with the goal of developing a power-efficient optical NoC. Planar structure of Panzer is shown in Fig. 22.

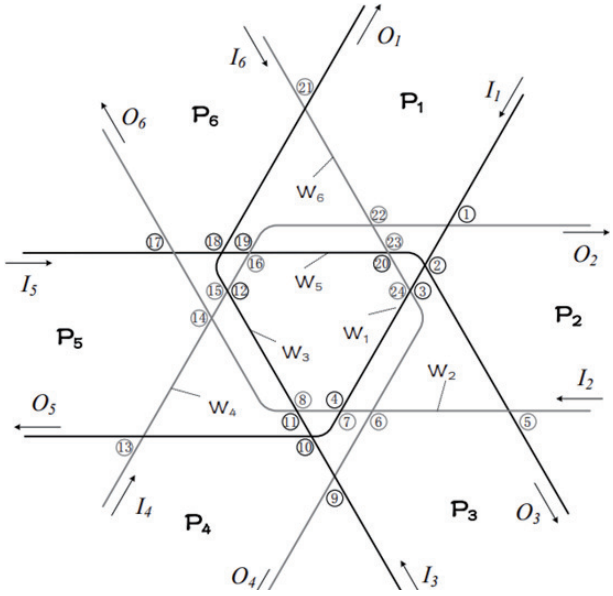

Fig. 22. Planar structure of Panzer[68].

Panzer employs a crossing angle of 60° or 120°, instead of the conventional 90°, to minimize crosstalk. A control unit configures all active MRs, which can switch between on/off states to control the drop or transmission of optical signals. When powered on, an MR enables the coupling of incident light with the resonance wavelength to another waveguide, while when powered off, the incident light continues along its original waveguide. The 6 × 6 Panzer router, consisting of 24 MRs and 6 waveguides with a 120° bending angle, has six ports, each with an input and output port. The waveguides connect the input ports to the output ports, with the MRs managing signal routing.

The authors of Ref. [69] proposed the Waffle router architecture, a novel design based on small 2 × 2 hybrid photonic–plasmonic switching elements that utilize microring resonators (MRRs). The architecture is named "waffle" due to its visual resemblance to a waffle pancake. It operates using a hybrid photonic–plasmonic switch composed of three components: two bus waveguides, a switching material, and MRRs. The switch functions by adjusting the bias voltage applied to the index tunable active layer (ITO layer) through a control unit, which alters the carrier concentration in the ITO layer. This adjustment allows the switch to toggle between two states: cross and bar. In the cross state, with zero bias voltage, optical signals can pass through the switching material to the opposing waveguides. When a suitable bias voltage is applied, the switch transitions to the BAR state, directing optical signals from an input port to the corresponding output port on the same waveguide.

The waffle architecture comprises 25 switching elements arranged in a 5 × 5 array, alongside 18 waveguides. each of the five ports (north, south, west, east, and local) features both an input and an output port. The switching elements are numbered from 1 to 25, with odd numbered elements positioned in the northeast direction and even numbered elements in the northwest direction. This arrangement ensures that internal paths are exclusively vertical or horizontal, optimizing space efficiency and symmetry. The ten ports are evenly distributed along the four sides of the router, which minimizes waveguide crossings by avoiding the concentra-

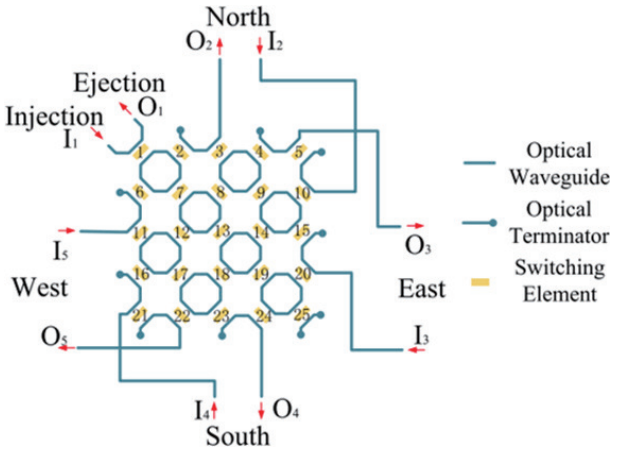

Fig. 23. (Color online) Waffle optical router architecture[69].

tion of input and output ports on the West and South sides. The Waffle architecture is illustrated in Fig. 23.

From a top-down perspective, the 25 switch elements and waveguides create 10 internal paths-5 input and 5 output paths. Each input path intersects with the 5 output paths individually, with a switch element at each crossing to control the direction of optical signals. The architecture features only two waveguide crossings, one between ports 4 and 5, and another between ports 8 and 9. Communication between any input and output port requires the use of only one switching element in the bar state, contributing to energy efficiency.

The XY routing algorithm is employed in the Waffle router due to its simplicity and its ability to prevent live lock and deadlock in 2D mesh-like topologies. This algorithm routes each packet along the horizontal axis until it reaches the destination column, after which the packet moves vertically to the destination node, without allowing turns from the Y dimension to the X dimension. To further optimize the architecture, some switching elements are replaced with crossings, resulting in the Waffle XY design. Theoretical analysis indicates that both Waffle and Waffle XY outperform several existing routers, particularly in terms of insertion loss and overall performance. Both designs are strictly non-blocking, making them suitable for mesh like networks.

In the realm of photonic integrated on-chip networks, the design of optical routers based on photonic crystals has garnered significant interest. The characteristics of these routers are detailed in Ref. [70], with a focus on how adjusting the crystal radius and materials broadens the scope of investigation. Materials such as germanium (Ge) with a refractive index (RI) of 4.0029, gallium arsenide (GaAs) with an RI of 3.3219, and indium phosphate (InP) with an RI of 3.457 are used in the construction of these routers. Performance evaluations are conducted within the wavelength range of 1500–1600 nm, and the routed wavelengths are systematically analyzed. Among the various configurations, Ge pillared routers exhibit the lowest levels of crosstalk and insertion loss.

The integration of ultra compact devices into the field of integrated photonics has further advanced the development of small sized routers, measuring just 33 μm × 36 μm. Simulations of photonic crystal-based wavelength routers are performed across the 1500–1600 nm wavelength range, utilizing FDTD and PWE techniques to enhance multicast routing efficiency. These routers, designed for multi core processors on a single chip, demonstrate excellent transmission capabilities across multiple wavelengths with minimal crosstalk and insertion loss. Notably, Ge and InP pillared routers show the lowest crosstalk and insertion loss, making them ideal for high-speed data transmission in multi core systems. Their ultra compact design also facilitates easy integration onto miniaturized chips

This paper[71] introduces a non-blocking four port photonic router designed specifically for the surix 2D mesh topology, aimed at enhancing physical layer and network performance parameters within multi core network topologies. To address challenges related to photonic insertion loss and power consumption, a novel Surix routing algorithm is proposed. This algorithm utilizes a control model and a circuit switching approach to optimize route selection, thereby minimizing both insertion loss and power usage between source and destination nodes.

Simulation results demonstrate that Surix outperforms traditional routers in network performance. Specifically, in the mesh topology, Surix shows a significant improvement in insertion loss, ranging from 9.92% to 37.15% compared to conventional routers. Among the tested algorithms, the west first and odd even algorithms, as well as the mesh network itself, result in the lowest levels of loss and power consumption when used with the Surix router. Conversely, the XY algorithm exhibits the highest levels of loss and power consumption. The surix router architecture is shown in Fig. 24.

These findings underscore the advantages of Surix in reducing both loss and power consumption, thereby enhancing network performance parameters in multi core network topologies. The Surix router design includes eight 1 × 2 parallel photonic switch elements (PSEs) and fourteen waveguide crossings, where one waveguide intersects with another. As Surix connects each input port to each output port, it supports the application of various routing algorithms. The proposed routing algorithm for Surix is specifically designed to select optimal routes between source and destination nodes, prioritizing minimal insertion loss and power consumption.

Researchers in Ref. [72] have a strong interest in ensuring the reliability of optical routers, as it directly impacts the efficiency of network operations. To address this concern, this study proposes a general technique that can be easily integrated into optical routers without introducing additional congestion or blocking issues. The technique involves implementing a reliable ring waveguide (RRW) with 2n microring resonators (MRs) in any $n \times n$ optical router. Notably, signals transmitted via the backup path do not interfere with those using the original path, underscoring a critical advantage of this approach.

To validate the effectiveness of the proposed method, a simultaneous transmission analysis was conducted on optical routers. The results indicate that RRW based optical routers exhibit a failure probability of no more than 5.19%, compared to 5.79% for FTTDOR. Additionally, RRW based routers demonstrate a significant increase in simultaneous transmission, ranging from 10% to 46%, when compared to FT-OXY and NRFT. The architecture of clockwise RRW is shown in Fig. 25.

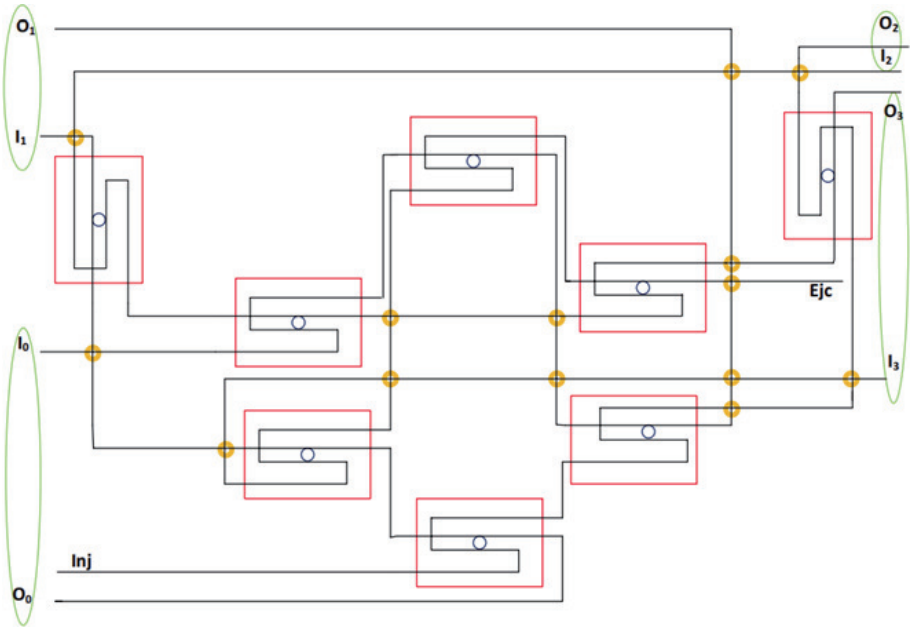

Fig. 24. (Color online) Surix optical router[71].

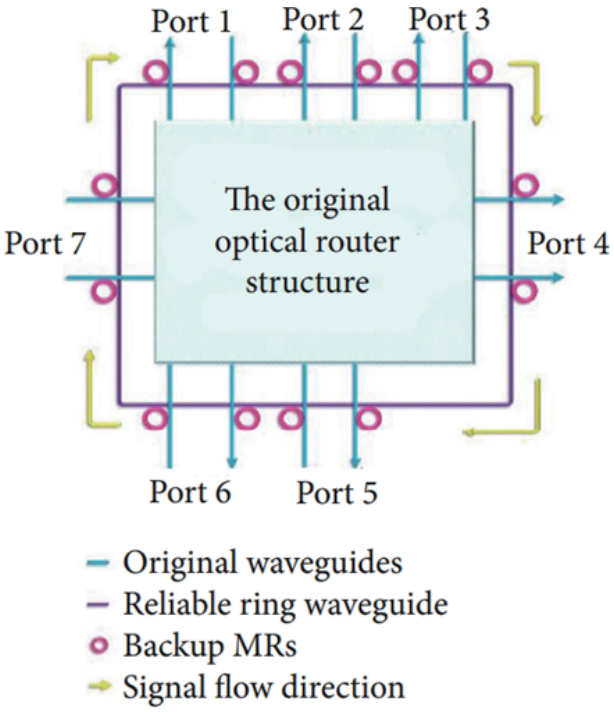

Fig. 25. (Color online) The reliable ring waveguide architecture of clockwise RRW[72].

A case study assessing the RRW scheme's implementation on a well-known optical router produced results closely resembling practical fabrication. Using the VPI photonics design suite (VPI), it was observed that implementing RRW results in a slight increase of −0.5 dB in the worst-case insertion loss for the default path, while the backup path experiences a slightly higher increase of −1.5 dB compared to the original router's default path. Additionally, RRW-based routers show a maximum decrease of 30.2% in worst-case insertion loss for 5 × 5 optical routers and 46.34% for 7 × 7 routers.

In terms of crosstalk noise, RRW-based architectures demonstrate significant improvements over FTTDOR and FT-Crux. The RO-Uni configuration reduces the worst-case crosstalk noise by 24.55% for the default path and 39.9% for the backup path. Similarly, the RRW-Crux configuration reduces crosstalk noise by 46.7% for the default path and 15.7% for the backup path compared to FT-Crux.

In various 2D mesh configurations, such as 4 × 4, 6 × 6, 8 × 8, 10 × 10, and 12 × 12, RRW-Crux significantly enhances the optical signal-to-noise ratio (OSNR). On average, the OSNR increases by 68.5% for the default path and by 15.9% for the backup path compared to FT-Crux.

To further improve network reliability, the authors plan to integrate the architectural design with a routing algorithm in future research.

This work, presented in Ref. [73], describes the design and analysis of a photonic routing network on chips using a non-blocking microring resonator based optical switched router. The optical router design features sixteen microring resonators, fourteen waveguide crossings, and four 90° waveguide bends, all of which can be tuned via thermos-optical (TO) or electro-optical (EO) effects. The researchers developed and evaluated a five port spatially non-blocking optical router with five input and five output ports to enable bidirectional communication. The sixteen microring resonators operate at the same resonance wavelength and are controlled by an on-chip electronic circuit. Their identical structural parameters streamline the fabrication process compared to wavelength selecting networks.

In this design, none of the four port compass directions can connect to themselves. Each of the twenty-one optical links is either established through a specific resonant microring or directly via a waveguide (where 'none' denotes no microring is required). Unlike metal track interconnects, photonic circuits can leverage optical waveguide crossings, allowing for complex routing within a 2D layer. However, crossings and bends introduce additional transmission loss, reflection loss, and crosstalk. Therefore, it is essential to design the router topology to minimize the number of crossings and bends, with a preference for reducing bends due to their higher associated loss. The proposed router architecture is shown in Fig. 26.

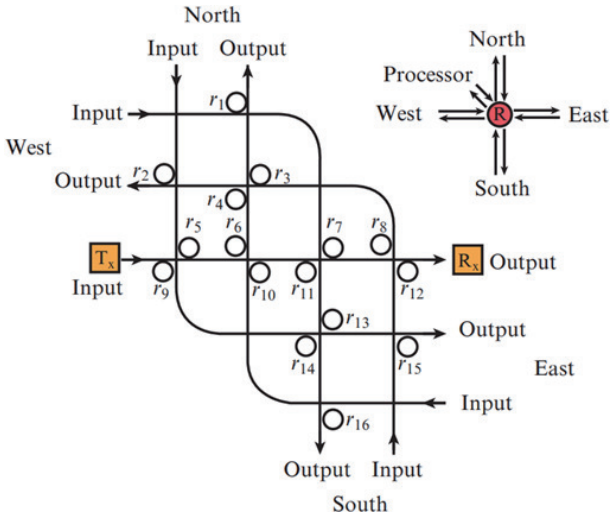

Fig. 26. (Color online) Proposed router architecture[73].

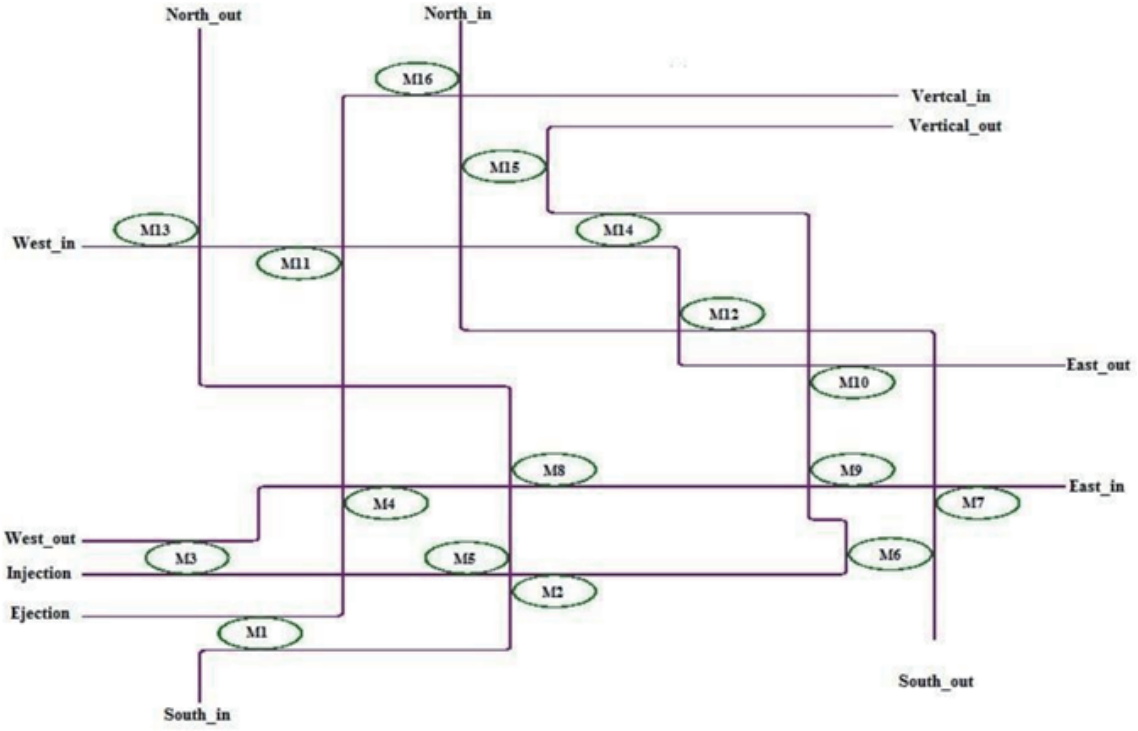

Fig. 27. (Color online) The proposed 6 × 6 optical router[74].

The proposed five port optical router, featuring sixteen microring resonators, fourteen crossings, and four bends, demonstrates a lower number of crossings, bends, and microring resonators compared to other routers. This reduction leads to decreased insertion loss, crosstalk, and enhances the scalability of photonic NoC. Furthermore, fewer microring resonators contribute to a reduction in device area and power consumption, although this does not affect optical links that use waveguides without microring resonators (e.g., the east to north link), which consume no additional power. The integration of four 90° waveguide bends and sixteen microrings results in a more compact design with faster switching speed, lower loss, and reduced optical power consumption compared to previously described 5 × 5 optical switching routers. Overall, the proposed optical router offers a promising approach for developing efficient and scalable photonic routing networks on chips.

Multilayer multi-core processors are increasingly in demand due to the need for more cores on a chip. Certain applications necessitate the use of 3D optical NoC (ONoC) architectures, which require advanced optical routers. In their paper[74], the authors introduce a 6 × 6 non-blocking optical router based on microring resonators (MRRs) that minimizes waveguide bending and crossing. The proposed optical router demonstrates the lowest insertion loss among existing non-blocking optical routers for 3D ONoC. Key design goals include reducing the number of MRRs, waveguide bendings, and waveguide crossings. Specifically, the design achieves 15 waveguide crossings, 18 waveguide bendings, and utilizes 16 MRRs. The proposed router architecture is shown in Fig. 27.

The proposed design leads to a 3 percent improvement in average insertion loss compared to current optical routers in 3D ONoC architectures. The reduced insertion loss signifi-

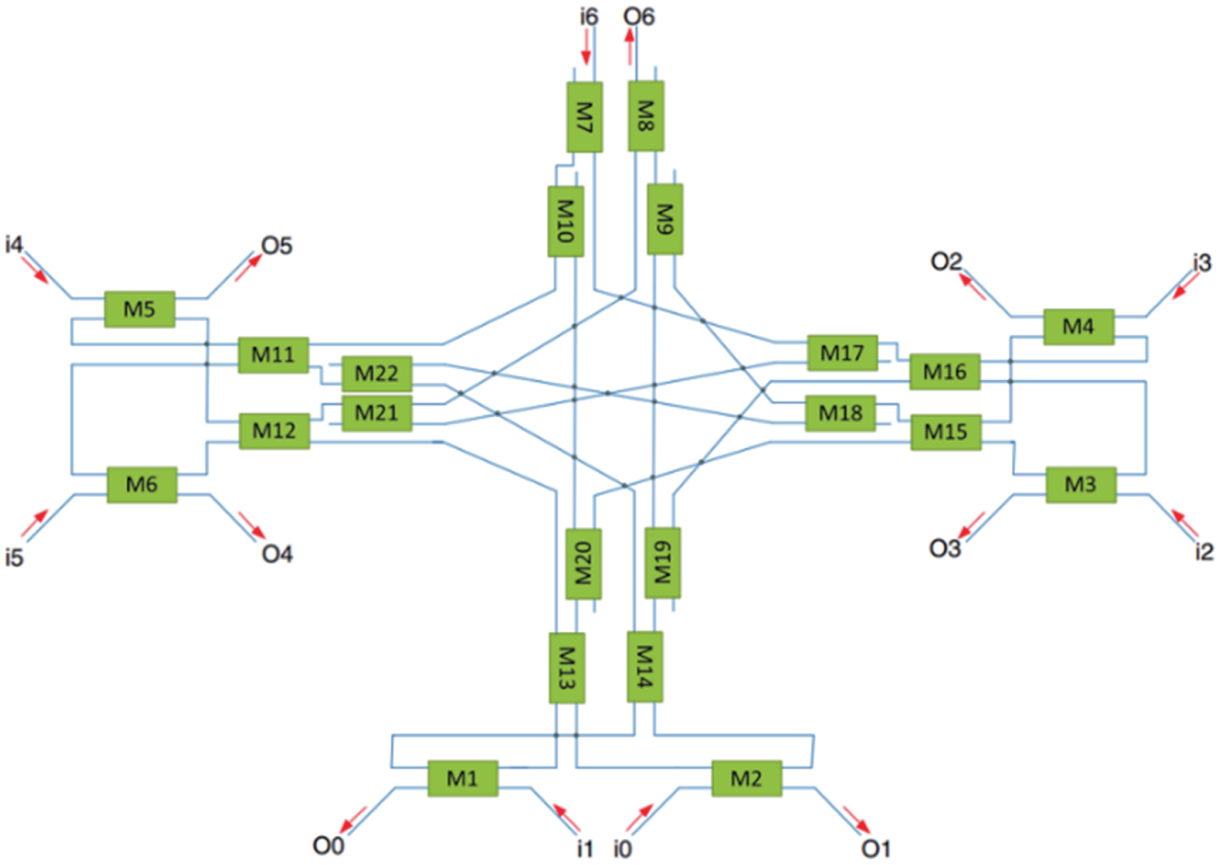

Fig. 28. (Color online) The design of a seven port optical router with 22 MZI based switching[75].

cantly enhances the ONoC performance. The 6 × 6 optical router, optimized by eliminating redundant routing paths (e.g., from 'south' and 'north' ports to 'east' and 'west' ports), utilizes MRRs as either cross switching elements (CSEs) or parallel switching elements (PSEs) through a microring and two waveguides. The implementation of an XYZ dimension order routing algorithm, which avoids these redundant paths, reduces the number of required MRRs to 16. This reduction leads to lower insertion loss, decreased power consumption, and a more compact design. The minimized number of waveguide crossings (15) and bendings (18) reduces crosstalk noise and loss, which are significant contributors to insertion loss in optical routers.

6.3. MZI-based optical routers

This study focuses on designing high throughput photonic NoC using MZI switches[75]. Compared to existing designs based on microring resonators (MRRs), the proposed MZI based routers exhibit superior performance, characterized by fewer switching elements, reduced waveguide crossings, and enhanced data transmission speed. The six port optical router features 12 switching elements, while the seven port router includes 22 elements.

The performance of these MZI based routers is notably superior to MRR based designs, with reductions in both switching elements and waveguide crossings. Insertion loss varies across optical paths, particularly when certain switches are in the bar state. The worst-case bit error ratio (BER) ranges from 5.94934×10^{-12} to 1.49797×10^{-10} for the six port and seven port routers, respectively, while the minimum *Q*-factor is 6.78144 for the six port router and 6.29899 for the seven port router. In optimal conditions, the minimum BER is 2.27966×10^{-12}, and the maximum *Q*-factor is 6.91866 for both router configurations. The power budget parameter, based on minimum transmitting power and receiving sensitivity, is 23 dBm. Successful transmission of a 20 Gbps optical signal through the routers was achieved.

The reduced number of switching elements and waveguide crossings leads to improved performance by minimizing losses and crosstalk. Integration of advanced optical router design techniques with the OptiSystem simulator has significantly optimized router performance and system design. This research advances photonic NoC, providing efficient and reliable data transmission in complex computing architectures. The streamlined designs for the six port and seven port optical routers facilitate high throughput optical interconnections in 3D mesh based NoC. The design of a seven port optical router with 22 MZI based switching is shown in Fig. 28.

The schematic layouts of the proposed optical routers are as follows: the six port optical router comprises 12 MZI based switching elements and 11 low loss waveguide crossings, while the seven port optical router includes 22 MZI based switching elements and 24 low loss waveguide crossings.

The authors described a 4 × 4 spatially non-blocking silicon photonic switch based on Mach–Zehnder interferometers in Ref. [76]. Fabricated using standard CMOS processes, this switch is compatible with existing technologies and operates across all 9 unique switch states, supporting 12 distinct input output routing configurations. It exhibits worst-case cross talk levels below –9 dB and has a common spectral bandwidth of 7 nm, ensuring reliable signal transmission. The

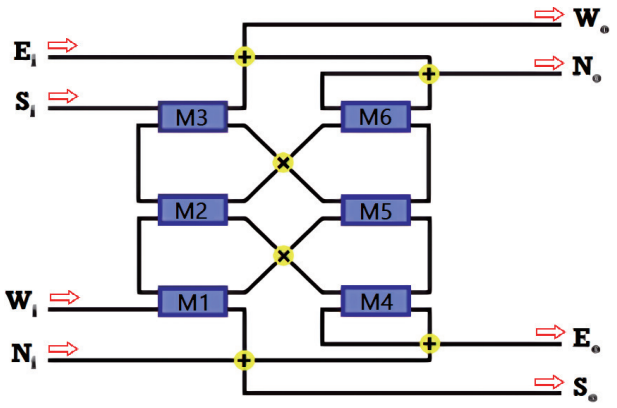

Fig. 29. (Color online) A 4 × 4 non-blocking photonic switch with six broadband 2 × 2 Mach–Zehnder based electro-optic switching components and six waveguide crossings is shown in the schematic[76].

steady state power consumption ranges from 7.4 to 20.4 mW, while the collective optical bandwidth for each switch state varies from 7 to over 120 nm. Cross talk between channels is better than −10 dB within the spectral range of 1524 to 1531 nm for most switch states. The extinction ratio is better than −25 dB in many states. The insertion loss of the switch ranges from 0.6 to 5.8 dB, depending on the switching state and I/O port. High-speed 40 Gbps data transmission experiments confirm the optical data integrity across all channels. The switch is capable of routing a 200 Gbps aggregate WDM signal while maintaining low energy consumption of 0.037 to 0.1 pJ/bit. This silicon photonic switch represents a significant advancement in optical switching technology, offering enhanced performance and compatibility with standard CMOS processes, making it suitable for various communication systems and networks. The proposed architecture is shown in Fig. 29.

The authors have developed a five port silicon optical router utilizing MZI switches[77]. The router, which incorporates 2 × 2 MZI switches, was fabricated alongside the optical components. Optical transmission spectra were measured with TE-polarized light from a tunable laser source. The device supports four transmission states, with spectra recorded for both the "off" and "on" states. The insertion loss of the switch is approximately 2.4 dB, primarily attributed to the 2 × 2 multimode interference (MMI) couplers. Optical crosstalk between ports is below −24 dB within the wavelength range of 1540–1580 nm.

Thermal tuning controls the MZI switches, which are configured in a symmetric setup with two 2 × 2 dB couplers and two 300 μm long phase shifters. The optical router comprises 10 switching elements, 5 waveguide crossings (with losses ranging from 0.2 to 0.3 dB per crossing), and MMI couplers with a width of 6 μm and length of 41.6 μm. The router operates within an optical bandwidth of 40 nm (1540 to 1580 nm). The total power consumption is 25 mW.

High speed data transmission tests revealed successful rates of 32 Gb/s through the router's 20 different input/output paths, with clear eye diagrams confirming signal integrity. However, some paths experienced increased noise due to additional losses from multiple MZI switches and a long straight waveguide. The router supports both thermal and electrical tuning, offering flexible switching capabilities with μs and ns switching times. The proposed architecture is shown in Fig. 30.

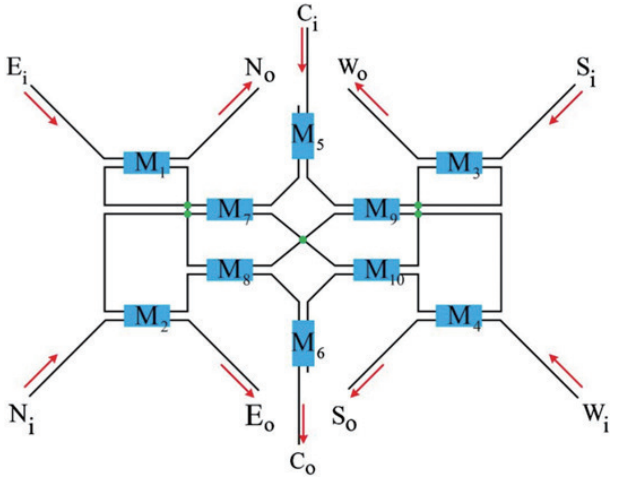

Fig. 30. (Color online) Diagram of a five port nonblocking optical router based on ten MZIs[77].

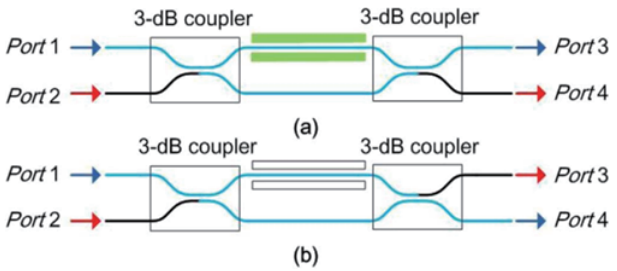

Fig. 31. (Color online) The diagram illustrates the configuration of a 2 × 2 Mach–Zehnder (M–Z) optical switch in two states: the "bar" status (a) and the "cross" status (b)[78].

The MZI based optical router shows considerable potential for on-chip optical interconnects, demonstrating effective high-speed data transmission and signal integrity. Future enhancements could include the integration of wavelength division multiplexing (WDM) technologies to further improve performance. Overall, the router's design is well suited for high-speed optical signal routing and can be refined to meet advanced application requirements.

The article titled "*N*-port strictly non-blocking optical router based on Mach–Zehnder optical switch for photonic networks-on-chip" explores the development of an *N*-port optical router designed for photonic NoC[78]. This study introduces a universal approach for constructing a strictly non-blocking *N*-port optical router using a 2 × 2 Mach–Zehnder optical switch. The analysis reveals the relationships between optical links from port *m* to port n and from port *m* to port $n - 1$, along with the connections between block matrices, underscoring the router's efficient routing capabilities. The strictly non-blocking nature of the *N*-port optical router is demonstrated using the contradiction method. Performance evaluations of simulated photonic NoC systems indicate that the optimal router dimension should not exceed 5 × 5. The proposed architecture is shown in Figs. 31(a) and 31(b).

The proposed *N*-port strictly non-blocking optical router, utilizing the Mach–Zehnder optical switch, offers several advantages. Its non-blocking architecture supports efficient and simultaneous communication between nodes, ensuring optimal data transmission. The router is scalable, allowing the

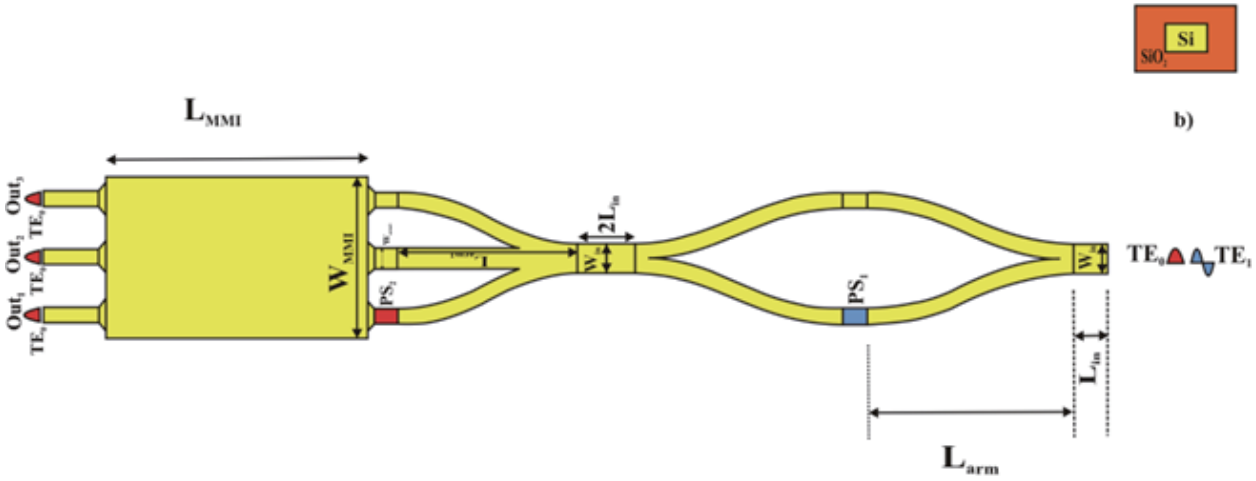

Fig. 32. (Color online) General diagram of two input-modes, three output-ports optical TE_0 mode router[79].

network to expand and meet increasing data transmission demands as the optical switch performance improves. Compared to previous designs, it shows enhanced performance in bandwidth utilization, transmission efficiency, and latency, thereby improving the overall performance of photonic NoC. This router provides a versatile and adaptable solution suitable for various network configurations, offering flexibility in designing photonic NoC.

However, the complexity of the router's design may present challenges in integration and manufacturing. Addressing power consumption is crucial for optimizing the router's efficiency and ensuring sustainable operation. Additionally, evaluating the implementation cost relative to the specific application and its benefits is important for practical deployment.

The Mach–Zehnder (MZ) optical switch, a key component of the router, can be fabricated on a silicon on insulator (SOI) wafer using the thermal-optical effect. Each MZ switch consumes approximately 104 mW of power. Electrodes, fabricated using techniques such as sputtering, ultraviolet photolithography, and dry etching, control the routing operation of the switch elements.

The router's design ensures non-blocking behavior by adhering to three rules: any input light can be directed to any output port, avoiding "U" turns, and not blocking potential optical links between other input and output ports. The scalability and versatility of the design are demonstrated through various embodiments for 4, 5, 6, and 8 port configurations, with each 2 × 2 MZ optical switch acting as an exchange node. By utilizing appropriate routing configurations and understanding the properties of fundamental optical links, the *N*-port optical router achieves efficient data flow between input and output ports.

For mode division multiplexing (MDM) systems, a novel design for a two input mode, three output port optical TE_0 mode router is proposed in Ref. [79]. This router facilitates the flexible routing of TE_0 or TE_1 input modes to the desired output ports with high efficiency and low crosstalk across the C-band. The device features a silicon based MZI and a multimode interferometer (MMI) to enable implementation in photonic integrated circuits (PICs). By appropriately configuring the two butterfly shaped phase shifters (PSs) at the MZI and MMI, the input mode—either TE_0 or TE_1—can be directed to one of the three output ports.

The design and optimization of the device utilize the three-dimensional beam propagation method (3D BPM). The device demonstrates exceptional performance, with insertion loss and crosstalk both below 0.4 dB and −24.5 dB, respectively, across the C-band. At a wavelength of 1550 nm, it achieves up to 99% efficiency and negligible crosstalk. The compact dimensions of the device (3.6, 634, and 0 μm) make it a promising candidate for high-speed multimode optical networks and on-chip optical integrated circuits. The proposed architecture is shown in Fig. 32.

The MZI consists of two 1 × 2 Y-junctions and has two branches (left and right) with a width (*W*_arm) designed to support only the TE_0 mode. It can either convert TE_0 to TE_1 or allow the input modes to pass through unchanged, depending on the phase shifter PS1's setting of 180 degrees or 0 degrees, respectively. The MZI output connects to a mode demultiplexer comprising a 1 × 3 Y-junction and a 3 × 3 MMI. The widths of the two side branches and the middle branch of the 1 × 3 Y-junction (W_arm and W_arm1) are chosen to exclusively support TE_0 mode.

The mode demultiplexer's three output ports connect to the three input ports of the 3 × 3 MMI. If the MZI output is TE_0 mode, it travels through the middle arm of the 1 × 3 Y-junction and reaches Out2. If the MZI output is TE_1 mode, adjusting PS2 to 90 or −90 degrees routes the signal to Out1 or Out3, respectively. The output mode is always converted to TE_0. The device is constructed using a ridge waveguide structure on an SOI platform, with the silicon core and silicon dioxide cladding having refractive indices of 3.47 and 1.44, respectively. Performance simulations are carried out using the 3D BPM method.

In Ref. [80], the authors propose a universal method for constructing an *N*-port non-blocking optical router using a 2 × 2 Mach–Zehnder optical switch, tailored for photonic NoC. They demonstrate that this optical router effectively achieves non-blocking functionality. The study confirms that the *N*-port optical router constructed with the Mach–Zehnder switch exhibits no blocking properties, establishing the approach as a generalizable solution for non-blocking optical routing.

In a separate study[81], the authors demonstrate the implementation of a highly versatile 4 port silicon thermo optic opti-

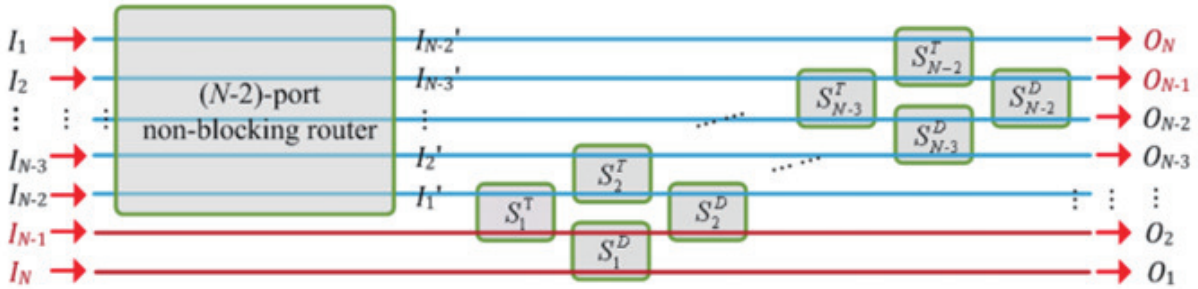

Fig. 33. (Color online) Expanding method from the (N – 2)-port non-blocking optical router to the N-port nonblocking optical router[83].

cal router utilizing Mach–Zehnder optical switches. This router exhibits reconfigurability and nonblocking characteristics, facilitating seamless routing operations. Notably, it maintains optical signal to noise ratios exceeding 15 dB for each optical link across its 9 distinct routing states within the wavelength range of 1525–1565 nm. The router's performance is further highlighted by its capability to manage 50 wavelength multiplexing channels per optical link, with each channel achieving a data rate of 32 Gbps within the specified wavelength range. Additionally, the router demonstrates a response time of approximately 19 ms, which enables it to swiftly adapt to dynamic network demands. In terms of energy efficiency, the router consumes an average of about 16.3 fJ/bit, reflecting its effectiveness in high performance data transmission.

The router's architecture includes four Mach–Zehnder (MZ) optical switches, designated as S1–S4, with four input ports (I1, I2, I3, I4) and four corresponding output ports (O1, O2, O3, O4). The MZ optical switch operates in two states: in the "bar" state, it directs incident light from input ports I1/I2 to output ports O1/O2, while in the "cross" state, it routes light from input ports I1/I2 to output ports O2/O1.

In the paper titled "a six port optical switch for cluster mesh photonic network-on-chip", the authors address the growing need for high performance multi core processors by introducing a novel non-blocking six port optical switch designed for cluster mesh photonic NoC systems[82]. To achieve this, they propose modifying the traditional Spanke Benes network by replacing three optical switching units with optical waveguide crossings. This modification reduces the number of optical switching units by 20% while maintaining routing path connectivity, leading to a reduction in both footprint and power consumption, although it may slightly affect network latency under certain conditions.

The implementation of the optical switch involves 12 thermally tuned silicon Mach–Zehnder optical switching units. The authors assess its theoretical spectral responses through a numerical model and further characterize its experimental spectral responses. The results indicate that the optical switch achieves optical signal to noise ratios (SNRs) greater than 13.5 dB across the wavelength range of 1525 to 1565 nm. Data transmission experiments demonstrate that the switch operates effectively at a data rate of 32 Gbps per optical link, showcasing its practical utility within the NoC framework.

The spanke benes architecture allows for 32 768 possible switching configurations. The proposed non-blocking six port optical switch supports 720 unique routing states, maintaining versatile routing capabilities. It successfully reduces the optical switching units to 12 while preserving 720 routing states. The propagation loss of the optical signal links ranges between 3.4 and 5.6 dB, and the optical SNR varies from 18.5 to 37.2 dB across different links and routing states. The extinction ratios of the measured eye diagrams for data transmission range from 16.4 to 17.7 dB, ensuring reliable signal integrity.

With an optical bandwidth spanning from 1525 to 1565 nm, the Mach–Zehnder optical switch supports WDM data transmission. The power consumption of the optical switching units ranges from 89 to 344.3 mW, depending on the routing state, which contributes to energy efficient operation. The optical switching unit features a response time characterized by a 10%–90% rise time of 11 μs and a 90%–10% fall time of 16 μs, ensuring rapid and reliable switching performance.

6.4. Hybrid optical routers

The authors present a universal method for constructing N-port non-blocking optical routers tailored for photonic NoC[83]. Their approach utilizes microring (MR) optical switches or Mach–Zehnder (M–Z) optical switches, each functioning as a 2 × 2 optical switch. This methodology leads to notable improvements in power consumption and reduces the number of optical switches required. Specifically, compared to previously reported MR based optical routers, their method achieves approximately a 50% reduction in the number of optical switches. When compared to M–Z optical switch-based routers, the authors' method results in a reduction of over 30% in the number of switches, thereby reducing the physical footprint and enhancing overall efficiency.

The authors provide a rigorous mathematical proof to validate the non-blocking routing capabilities of their proposed N-port optical routers. Detailed comparisons of insertion loss between their routers and reported alternatives further underscore the superiority of their approach. Their research offers a robust and scientifically sound method for constructing N-port non-blocking optical routers, optimized for photonic network architectures. By minimizing power consumption and optimizing optical switch usage, their method enhances performance and efficiency. The proposed architecture is shown in Fig. 33.

The functionality of non-blocking optical routers with 3 and 4 ports demonstrates their viability as building blocks for constructing N-port non-blocking optical routers using the expansion method. The expansion process involves adding two extra waveguides and 2(N – 2) optical switches to the existing (N – 2)-port router, thereby establishing optical links between the original N – 2 ports and the two new ports.

In a recent study[84], a 2 × 2 hybrid photonic–plasmonic switching (HPPS) based rearrangeable non-blocking 6 × 6 router (RoR) was introduced. This architecture features 15 HPPS elements distributed across 6 waveguides with 8 crossings. By optimizing the design and reducing the number of HPPS elements, the proposed architecture demonstrates superior performance in terms of insertion loss, crosstalk noise, and power consumption compared to unoptimized designs.

The reorganization of inputs and outputs within the optical router further enhances performance and reduces the footprint of the optimized RoR (oRoR). The HPPS elements function as the fundamental switching units, toggling between cross and bar states through a bias voltage controlled by a modulating unit. This adjustment alters the carrier concentration of the index tunable active (ITO) layer, directing the optical signal through specific waveguides based on input output requirements. The RoR consists of 15 basic 2 × 2 HPPS elements, offering 2^{15} possible switching states to meet the requirement of 720 distinct states. The proposed architecture is shown in Figs. 34(a)–34(e).

To enhance design efficiency, an optimization technique replaces some switching elements with straight waveguides and reconfigures inputs and outputs while maintaining the non-blocking capability and 720 routing states. This refined RoR (oRoR) achieves reduced insertion loss and power consumption while providing a more compact footprint. The optimized design outperforms contemporary router architectures by minimizing the number of switching elements, thus reducing complexity and improving efficiency.

Numerical results illustrate the advantages of the proposed design. The worst-case insertion loss for the oRoR in the R1 routing state is 20.5 dB, compared to 15.4 dB in the R2 and R6 states. The oRoR achieves an average insertion loss reduction of 18% to 42% relative to the RoR. The minimum best-case average insertion loss for the oRoR is 1.74 dB in the R4 routing state, while the worst-case average insertion loss for the RoR is 11.7 dB in the same state. Additionally, the worst-case crosstalk noise for the RoR in the R4 state is 3.25 dB, whereas it is 2.6 dB for the oRoR.

Comparative analysis shows that the oRoR architecture has the fewest switching elements and waveguide crossings among other 6 × 6 router designs, achieving up to a 50% reduction in switching element count. These results underscore the enhanced performance, efficiency, and reduced complexity of the oRoR design, highlighting its potential as a leading solution for advanced photonic–plasmonic switching in optical networks.

7. Results and discussions

To facilitate a comprehensive comparison of various optical router designs, a set of selected criteria has been chosen based on their critical importance in analyzing and characterizing these routers as presented in research papers. These criteria are fundamental in understanding key aspects and features of optical routers, enabling a detailed evaluation of different design approaches.

In the context of optical router design and comparison, it is important to note that not all research papers provide comprehensive information on all the selected criteria simultaneously. Some papers may focus on specific aspects or present only a subset of the criteria. Nevertheless, the criteria chosen for this comparison have been carefully selected due to their critical importance and significant impact on the functionality of optical routers. These criteria play a crucial role in determining the overall system throughput and performance of ONoC systems. They are fundamental factors that directly influence the router's efficiency, scalability, and ability to handle data streams effectively.

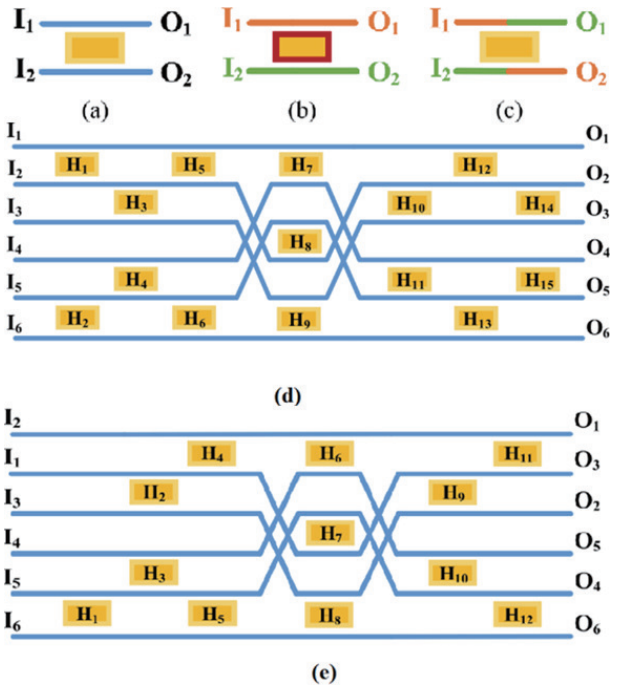

Fig. 34. (Color online) 2 × 2 HPPS Element (a). HPPS with applied voltage in the Bar state (b). HPPS without applied voltage in the Cross state (c). RoR with 15 HPPS elements (d). oRoR with 12 HPPS elements (e)[84].

By focusing on these criteria, we can gain valuable insights into the fundamental characteristics of routers and make meaningful comparisons between different designs. It is also worth noting that the selected criteria are often more extensively covered in research papers compared to other factors. This suggests that researchers have recognized their significance and have devoted efforts to investigating and presenting findings on these crucial aspects. Therefore, emphasizing these important criteria in the comparison provides a more comprehensive understanding of the strengths and limitations of various router designs, enabling informed decisions and advancements in the field of ONoC.

The selected criteria are essential for evaluating and optimizing optical routers. While other factors may contribute to overall performance, efficiency, or specific application requirements, the chosen criteria form the core elements that are consistently addressed in the majority of works. As a result, focusing on these criteria allows for a more efficient and meaningful evaluation of different router designs.

Type of router: this refers to the specific architecture or design approach employed in the construction of the optical router. Types may include microring resonator based routers, MZI based routers, hybrid designs, and their variations such as matrix switches or photonic crystal routers. Understanding the type of router provides insights into the underlying

Table 1. Microring resonator (MRR) routers survey criteria.

Reference	Type of router	Ports	Blocking/ non-blocking	Switching elements	MRRs	Waveguide crossings
[47]	Optical router with microring resonators (MRRs)	8	Blocking	64	8 × 8 MRR array	64
[48]	4-port router with 8 microring resonators	4	Non-blocking	4	8 MRRs	4
[49]	Non-blocking photonic switch	4	Non-blocking	4, 8	8	4
[50]	Microring-based optical switch	8	Non-blocking	192 switches	8 × 8 matrix switch	Not specified
[51]	Optical router based on OXY architecture	6 × 6, 9 × 9, and 12 × 12	Non-blocking	Not specified	6 × 6, 9 × 9, and 12 x 12	Not specified
[52]	Cascaded microring resonator-based optical switch	5	Non-blocking	10	25	25
[53]	Matrix switch	5	Non-blocking	25	25 MRRs	25 multimode-interference-based crossings
[54]	Router design	12	Non-blocking	12	12 MRRs	19 crossings
[55]	Optical router design	4	Non-blocking	8	8 MRRs	6 crossings
[56]	Optical router design	4 and 5	Non-blocking	25	25	10
[57]	Generic technique for non-blocking optical routers	$N \times N$	Non-blocking	$N(N-2)$	$N(N-2)$	N
[58]	Helix-h switch design	4	Non-blocking	8	8	8 crossings
[59]	Cygnus optical router	5	Non-blocking	25 (silicon micro-resonators)	25 (silicon micro-resonators)	$2N$
[60]	Generic wavelength-routed optical router (GWOR)	4	Non-blocking	$N(N-2)$, $(N-1)2$	$N(N-2)$, $(N-1)2$	$N-1$
[61]	Five-port optical router design	5	Non-blocking	16 MRRs	16 MRRs	Four bends and fourteen crossings
[62]	Photonic crystal ring resonator (PCRR) based 6 × 6	6	Not specified	24	24 PCRRs	24 PCRRs
[63]	7 × 7 non-blocking optical router	7	Non-blocking	Not specified	Not specified	Not specified
[64]	Five-port spatially non-blocking optical router	5	Non-blocking	Not specified	16 MRRs	14 crossings
[65]	8 × 8 optical router	2, 8	Not specified	Not specified	Not specified	Not specified
[66]	Odor (optical dimension order router)	6	Not specified	Not specified	Not specified	Not specified
[67]	Five-port non-blocking optical networks-on-chip (ONoC) router	5	Non-blocking	Not specified	Not specified	Not specified
[68]	6 × 6 optical router called Panzer	6	Not specified	Not specified	Not specified	Not specified
[69]	Waffle router architecture	5	Non-blocking	25	20	2
[70]	Photonic crystal-based routers	4	Not specified	8	8	10
[71]	Four-port photonic router for Surix 2-D mesh topology	4	Non-blocking	8	8	14
[72]	6 × 6 non-blocking optical router	6	Non-blocking	Not specified	$2n$	15 crossings
[73]	Non-blocking microring resonator-based optical switched router	N	Non-blocking	$N(N-2)$	16 MRRs	14 crossings
[74]	6 × 6 non-blocking optical router	6	Not specified	15	15	15 crossings

principles and methodologies used in its design.

Number of Ports: this criterion refers to the total number of input and output channels available in the optical router. It provides valuable information about the router's capacity to handle simultaneous data streams and its potential for scalability in larger network configurations.

Blocking or non-blocking: this determines whether the optical router operates in a blocking or non-blocking manner. A non-blocking router can establish connections between any input and output ports simultaneously, ensuring uninterrupted data transmission. In contrast, a blocking router may experience contention or restrictions in establishing certain connections.

Number of switching elements: this represents the count of individual components responsible for routing and switching data within the optical router. These elements can include microring resonators, MZIs, hybrid switches, or other switching technologies. Understanding the number of switching elements provides insights into the router's complexity and potential scalability.

Waveguide crossings: this criterion refers to the points in the optical router where waveguides intersect or cross paths. The number of waveguide crossings is critical as it directly influences signal integrity, crosstalk, and overall performance. A higher number of crossings may introduce signal degradation and complexity.

The subsequent sections will present and compare these criteria and characteristics for routers based on microring resonators, Mach–Zehnder interferometers, and hybrid designs.

Table 2. Mach–zehnder (MZI) routers survey criteria.

Reference	Type of router	Ports	Blocking/non-blocking	Switching elements	Waveguide crossings
[75]	Six-port optical router, seven-port router	Six, seven	Non-blocking	12 (six-port), 22 (seven-port)	Not mentioned
[76]	4 × 4 electro-optic silicon switch	*N*-port	Non-blocking	*N*-port	2, 4, and 0
[77]	Five-port silicon router	Five	Blocking	10	5
[78]	*N*-port optical router	*N*-port	Non-blocking	15 MZI, 24 MZI ,48 MZI	No waveguide crossing in the proposed 5-port optical router
[79]	Two-input-mode, three-output-port router	Three	Not mentioned	Not mentioned	Not mentioned
[80]	*N*-port optical router	*N*-port	Non-blocking	Not mentioned	Not mentioned
[81]	Versatile 4-port configuration	Four	Non-blocking	Four (MZ switches)	Not mentioned
[82]	Six-port optical switch	Six	Non-blocking	12	Not mentioned

7.1. MRR architecture comparative results

The Microring Resonator (MRR) architecture is a notable category of optical NoC routers, distinguished by its unique properties and advantages. MRR routers leverage the phenomenon of resonant coupling in microring resonators to facilitate efficient data routing and transmission within the NoC framework.

One of the primary advantages of MRR routers is their compact size and low power consumption. The small footprint of MRRs allows for a higher integration density, enabling the implementation of numerous MRR based routers on a single chip. Additionally, MRRs are energy efficient due to their passive nature, contributing to low power consumption for on-chip communication.

Another significant benefit of MRR routers is their inherent wavelength selectivity, which supports WDM techniques. By utilizing different wavelengths for data transmission, MRR routers can enhance overall data capacity and improve network throughput.

However, MRR routers also face certain limitations and challenges. A key drawback is the limited number of available wavelengths for routing, which can constrain the scalability of the system. Additionally, MRRs are sensitive to environmental variations, such as temperature fluctuations, which can impact their performance and stability. Achieving precise control and tuning of MRRs presents another challenge, requiring advanced control mechanisms and calibration techniques.

Despite these challenges, MRR routers offer substantial advantages in terms of size, power consumption, and wavelength selectivity, making them a promising solution for optical NoC systems. Ongoing research aims to address scalability issues and improve the performance and reliability of MRR based routers, with the goal of unlocking their full potential in future on-chip communication architectures. Table 1 displays the survey criteria for routers that utilize microring resonators (MRRs).

7.2. MZI architecture comparative results

The MZI architecture is a prominent category of optical NoC routers. MZI routers offer several advantages that make them a compelling choice for on-chip communication. Firstly, MZI routers are capable of performing both wavelength routing and switching, which facilitates efficient WDM data transmission. This capability enhances bandwidth utilization and increases data transfer rates within the NoC framework. Additionally, MZI routers exhibit low crosstalk due to their inherent optical isolation properties, helping to maintain signal integrity and minimize interference between channels. Moreover, MZI routers are highly scalable; they can be expanded to accommodate a larger number of input and output ports without significant performance degradation.

However, MZI routers also have some drawbacks. A primary challenge is the complex control circuitry needed to configure and manage the routing paths within the MZI router. This complexity can lead to increased power consumption and design challenges. Additionally, MZI routers are sensitive to temperature variations, which can impact their performance and potentially degrade signal quality. Despite these limitations, the MZI architecture remains a promising solution for optical NoC routers, especially in scenarios where wavelength routing, low crosstalk, and scalability are critical requirements. Table 2 provides a comprehensive breakdown of each work.

7.3. Hybrid architecture comparative results

In addition to the comparative analysis presented, it is important to recognize that selecting the best optical router design depends on the specific constraints and requirements of the application. Each router architecture has its own set of advantages and disadvantages, as highlighted in the survey. Researchers and designers must carefully consider these factors and align them with their design objectives. Table 3 provides a comprehensive breakdown of each work based on the survey criteria for hybrid routers.

The survey provides valuable insights into the characteristics and performance of different router architectures, allowing for a comprehensive evaluation of their strengths and limitations. However, it is essential to understand that the survey focuses on presenting these advantages and disadvantages rather than determining the absolute best design. Designers need to consider various factors such as power consumption, scalability, crosstalk, signal integrity, and environmental sensitivity to make informed decisions.

The survey serves as a valuable resource by offering a thorough understanding of different architectures, enabling researchers to assess their suitability and make well-informed choices based on specific design constraints and requirements. Ultimately, selecting the optimal router design involves careful consideration of the trade-offs and compromises between various criteria. By leveraging insights from the survey and conducting further research, designers can

Table 3. Hybrid routers survey criteria.

Reference	Type of router	Ports	Switching elements	ports	Blocking/non-blocking	Waveguide crossings
[83]	2 × 2 router architecture	*N*-port optical router is used as a (*N* − 1)-port optical router.	4 optical switches (4-port router), 8 optical switches (5-port router)	4-port and 5-port	Non-blocking	Not mentioned
[84]	6 × 6 hybrid photonic-plasmonic switching (HPPS) router architecture	2 × 2 hybrid photonic-plasmonic switching (HPPS)-based rearrangeable non-blocking 6 × 6 rout	15 HPPS elements (RoR architecture), 12 HPPS elements (oRoR architecture)	6-port	Non-blocking	Eight crossings using six waveguides

develop innovative and efficient optical router solutions tailored to their specific application needs.

8. Challenges and future directions in optical router design

The advancement of optical ONoC technology underscores several critical challenges and opportunities for future research, particularly in the domain of optical router design. This section explores these challenges in depth and proposes targeted research directions to address them, ensuring a thorough and insightful discussion beyond a mere summary of existing literature.

8.1. Major challenges

Scalability and integration: As the number of cores on a chip continues to rise, optical routers must scale to manage the increasing data throughput and complex routing demands. The challenge lies not only in handling the high data rates but also in integrating these optical routers with existing CMOS technologies. This integration is crucial for hybrid systems that combine optical and electronic components. Achieving seamless integration requires innovations in both optical and electronic design to ensure that the benefits of optical communication, such as high bandwidth and low latency, are fully realized without compromising the performance of electronic components. The design must accommodate the physical constraints of chip architecture while providing robust routing capabilities to handle growing core counts and data traffic efficiently[85].

8.2. Thermal management

Optical routers generate significant amounts of heat during operation, which can adversely affect their performance and longevity. Effective thermal management is essential to prevent overheating, which can lead to signal degradation, reduced reliability, and potential failure of optical components. Advanced cooling solutions and innovative thermal management strategies are needed to address this issue. These may include the development of new materials with high thermal conductivity, improved heat dissipation techniques, and the integration of micro-cooling systems to maintain optimal operating temperatures. Addressing thermal management challenges is critical for ensuring the stable operation and extended lifespan of optical routers in high-performance computing environment[86].

The fabrication of optical routers involves complex processes that can be expensive, particularly due to the high-cost materials and intricate manufacturing techniques required for photonic devices. Reducing fabrication costs while maintaining high performance is a significant challenge. Innovations in manufacturing technologies, such as advanced photolithography techniques, cost-effective material alternatives, and scalable production methods, are necessary to make optical routers more commercially viable. Developing more affordable and efficient fabrication processes will be key to enabling widespread adoption of optical routers and advancing the field of optical networks[87].

The integration of optical components with CMOS technology presents technical difficulties that need to be overcome to create hybrid systems that leverage the advantages of both optical and electronic components. This integration involves ensuring compatibility between photonic devices and electronic circuits, managing signal interfaces, and addressing issues related to impedance matching and power consumption. Research into novel integration techniques, such as hybrid integration platforms and advanced packaging methods, is crucial for achieving seamless operation between optical and electronic components. Successful integration will enhance the overall performance and functionality of optical NoC.

Developing efficient routing algorithms and control mechanisms tailored for optical networks is essential for managing high-speed data transmission and dynamic network conditions. Optical networks require specialized algorithms that can handle the unique characteristics of optical communication, such as wavelength multiplexing and signal attenuation. These algorithms must optimize data paths, minimize latency, and adapt to changing network traffic patterns to ensure reliable and efficient data routing. Additionally, advanced control mechanisms are needed to manage network resources, handle congestion, and provide fault tolerance. Research in this area should focus on creating adaptive and scalable solutions that can meet the demands of future optical network architectures[88].

8.3. Future research directions

Research into novel materials, such as two-dimensional materials (e.g. graphene) and new photonic crystals, has the potential to significantly enhance the performance and cost-effectiveness of optical routers. These materials offer unique optical properties, such as high refractive indices and low loss, which can improve the efficiency of optical components and reduce fabrication costs[8]. The development of advanced materials can lead to the creation of more compact, efficient, and cost-effective optical routers, driving innovation in optical network technologies[89].

The development of advanced routing algorithms specifically designed for optical networks is crucial for optimizing data paths and managing network traffic. These algorithms should be capable of handling the high-speed and high-band-

width requirements of optical communication, as well as adapting to dynamic network conditions. Research should focus on creating algorithms that improve efficiency, reduce latency, and enhance network performance by leveraging the unique features of optical communication, such as WDM and optical switching[52]. Effective routing algorithms will play a key role in enabling the full potential of optical NoC[90].

Exploring hybrid architectures that integrate optical and electronic components can address scalability issues and improve overall system performance. Hybrid systems can combine the high bandwidth and low latency of optical communication with the processing power and flexibility of electronic circuits, creating a balanced solution for future computing systems. Research in this area should focus on developing integration techniques, optimizing system designs, and addressing challenges related to interfacing optical and electronic components. Hybrid architectures hold promise for overcoming the limitations of traditional electronic-only systems and advancing the capabilities of optical networks[91].

Addressing the thermal management challenges associated with optical routers is crucial for their reliable operation and extended lifespan. Research into advanced cooling techniques, such as microfluidic cooling and phase-change materials, as well as the development of new materials with high thermal conductivity, can help mitigate heat dissipation issues. Effective thermal management solutions will enhance the performance and reliability of optical routers, making them suitable for larger and more complex systems[92].

Interdisciplinary research that fosters collaboration among experts in photonics, electronics, and computer architecture is essential for overcoming existing challenges and driving innovation in optical router design. By combining expertise from different fields, researchers can develop novel solutions, address complex problems, and advance the state of the art in optical network technologies. Collaborative efforts will be crucial for accelerating progress and achieving breakthroughs in optical router design[93].

Establishing standards and benchmarks for evaluating optical routers can facilitate progress by providing a common framework for assessing performance and interoperability. Standardization will enable researchers and practitioners to compare different designs and technologies, identify best practices, and drive improvements in optical network systems. Developing comprehensive benchmarks will also support the validation and comparison of new approaches, contributing to the advancement of the field[94, 95].

Investigating emerging applications and use cases for optical routers can provide valuable insights into their potential impact and areas for development. Understanding how optical routers can address specific needs in data centers, high-performance computing, and other domains will guide future research and development efforts. Exploring new application areas can reveal opportunities for innovation and help drive the adoption of optical network technologies[94–96].

This comprehensive discussion of challenges and future research directions provides a thorough overview of the key issues and opportunities in optical router design, addressing the reviewer's comment and ensuring that the paper offers valuable insights and guidance for future research.

9. Conclusions

In conclusion, the emergence of ONoC technology offers a promising solution to address the limitations of traditional electronic interconnects, such as bandwidth constraints, high latency, and power consumption issues. Within ONoC design architectures, optical routers play a critical role by enabling high-speed, low-latency data transfer, efficient data routing, and meeting the scalability requirements of modern computing systems.

This study serves as an introductory resource for beginners, providing a fundamental understanding of ONoC and optical routers, while also offering a comprehensive survey and analysis for experts. It focuses on three main categories of router architectures: microring resonators (mrrs), MZIs, and hybrid designs. Additionally, the study provides insights into the specific advantages and limitations of these router architectures.

The MRR architecture, for example, offers advantages such as compact size, low power consumption, and wavelength selectivity. However, it faces challenges related to a limited number of available wavelengths and susceptibility to environmental variations. Conversely, the MZI architecture benefits from wavelength routing and low crosstalk but requires complex control circuitry and is sensitive to temperature fluctuations. Hybrid architectures, which combine the strengths of MRRs and MZIs, offer a flexible trade-off between power consumption and routing efficiency while maintaining scalability. However, they also introduce design complexities and may experience issues related to optical loss and crosstalk.

Selecting the optimal optical router design involves careful consideration of factors such as power consumption, scalability, crosstalk, signal integrity, and environmental sensitivity. The survey presented in this study provides valuable insights into the characteristics and performance of different router architectures, enabling researchers and designers to make informed decisions based on their specific design requirements and constraints. The comparative analysis and evaluation of these optical router architectures offer crucial insights into their strengths and limitations, helping to determine the best design based on specific constraints and application needs.

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